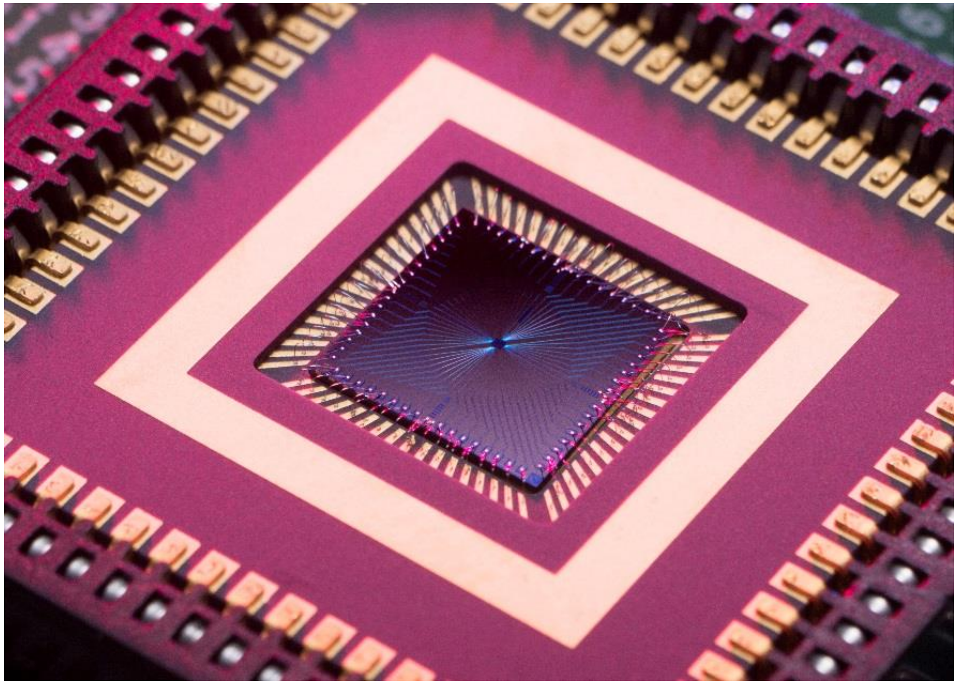
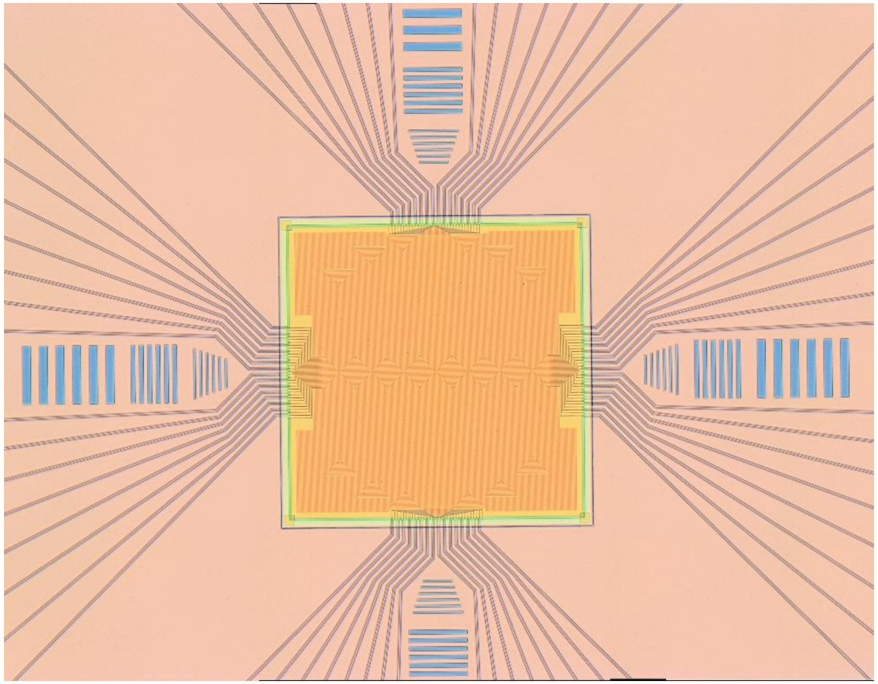
Superconducting Nanowire Single Photon Detectors for Optical Communication and Quantum Optics

Matt Shaw

MIT-LL, 4 April 2018

Jet Propulsion Laboratory, California Institute of Technology





JPL SNSPD Development Team

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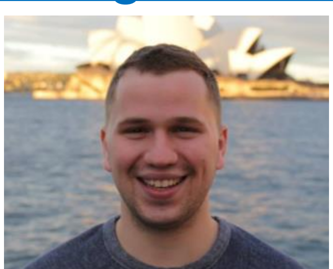
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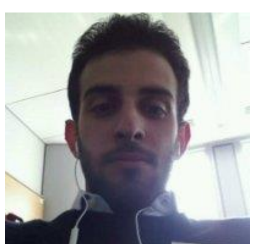
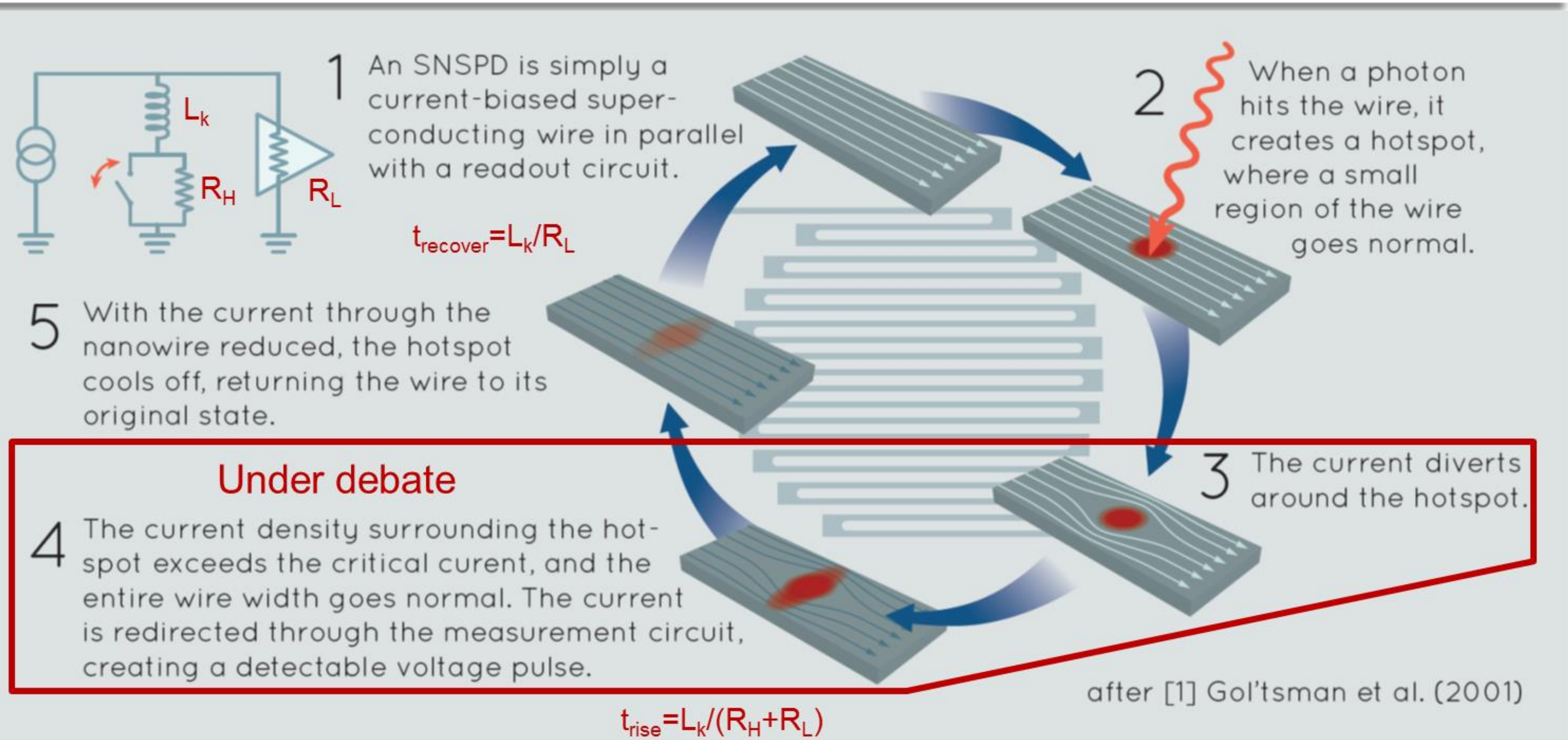

Simone Frasca


Eddy Ramirez

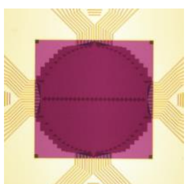
SNSPD Device Concept

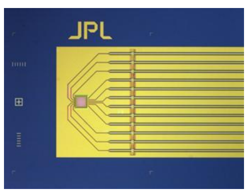


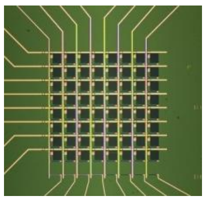
- Detection mechanism in SNSPDs is still an area of lively ongoing research
- Improved understanding of SNSPD device physics is essential to identifying fundamental limits of detector performance and engineering improved devices

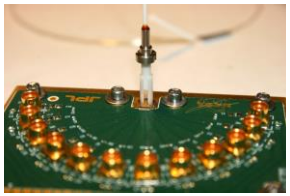
WSi IR Arrays for Optical Communication

- 64 pixel arrays for DSOC ground terminal
- 64 pixel imaging arrays with row-column readout
- 12 pixel arrays for secondary LLCD ground terminal
- Fiber-coupled arrays for QKD
- Feasibility studies for future ISS teleportation concept



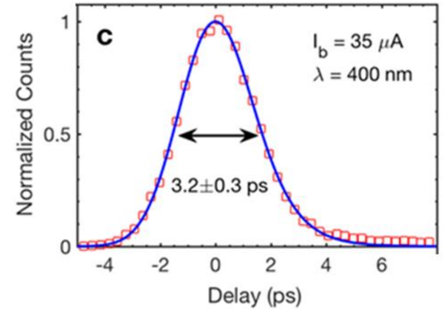


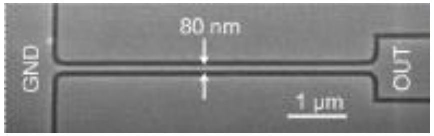




Ultra-high Timing Resolution

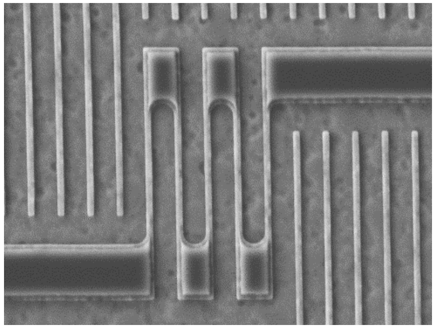
- 3.2 ps FWHM jitter in specialized NbN device
- 4.9 ps at 1550 nm
- 7.1 ps using WSi
- Close collaboration with MIT and NIST Boulder
- Techniques applied to large-area array yielded 25 ps FWHM

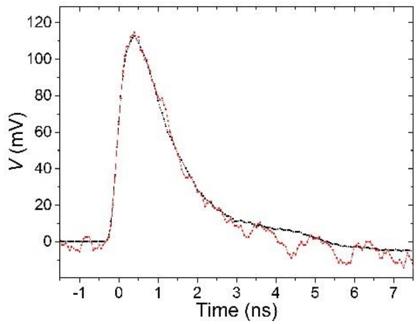




High Operating Temperature SNSPDs

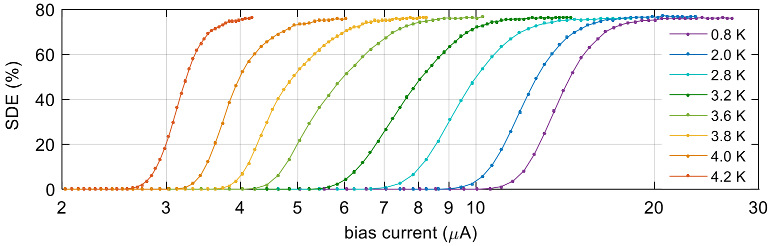
- MgB2 SNSPDs single photon sensitive at 17 K
- Considerable future development necessary



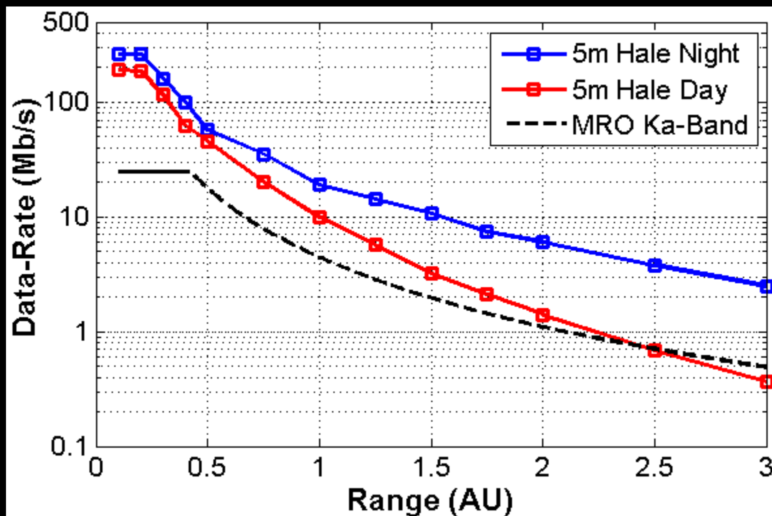


MoSi Ultraviolet SNSPDs

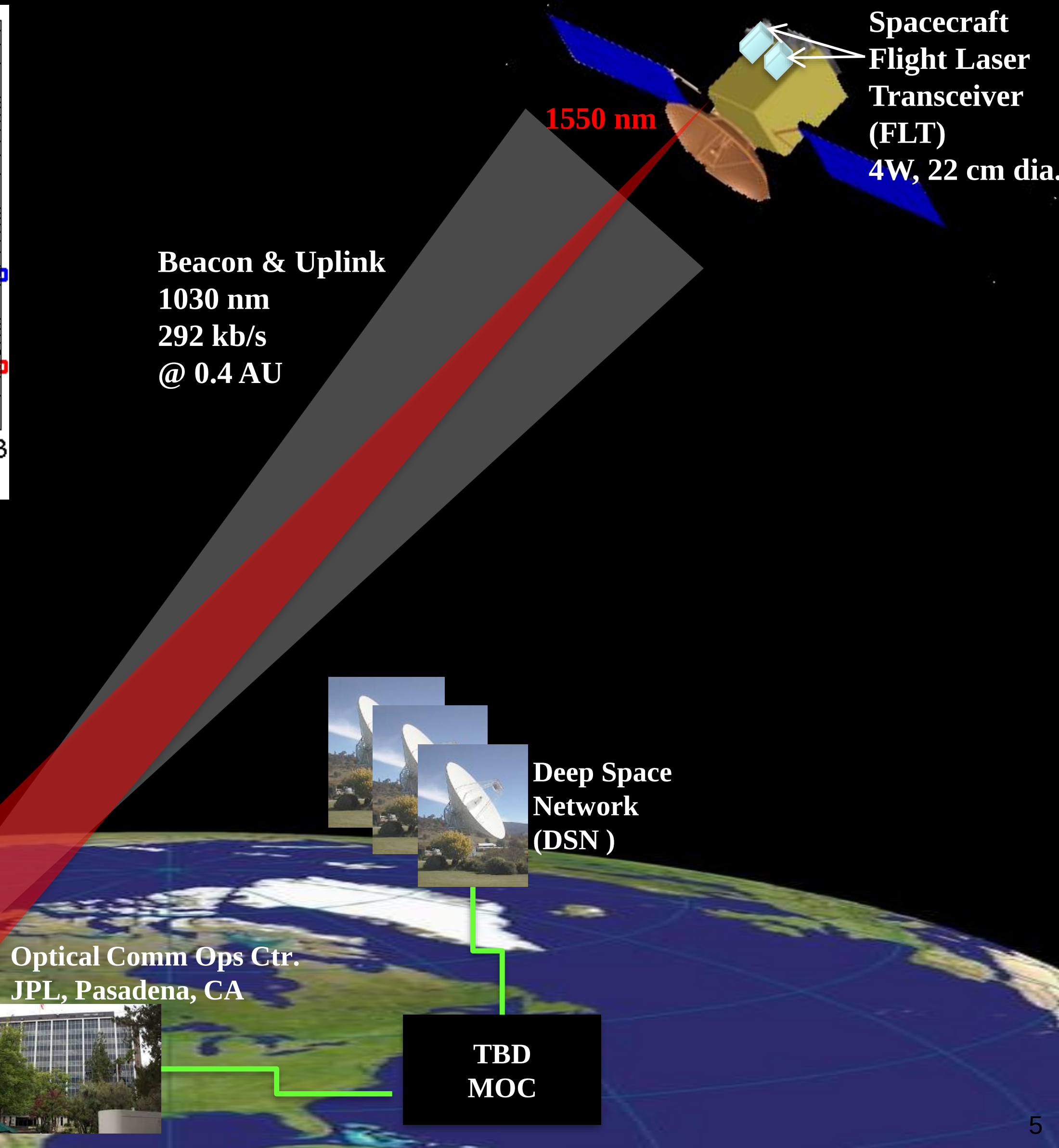
- UV SNSPDs for trapped ion quantum computing
- 80% efficiency at 370 and 315nm at 4.2 K
- Single photon sensitivity at 245nm
- Close collaboration with NIST, Duke, Sandia



DSOC Tech Demo Mission

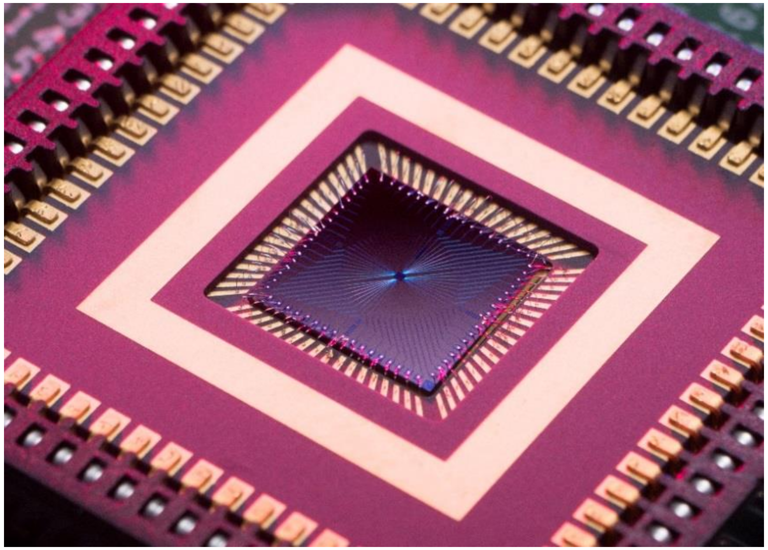


Performance using 4W average laser power w/22 cm flight transceiver to 5m ground telescope



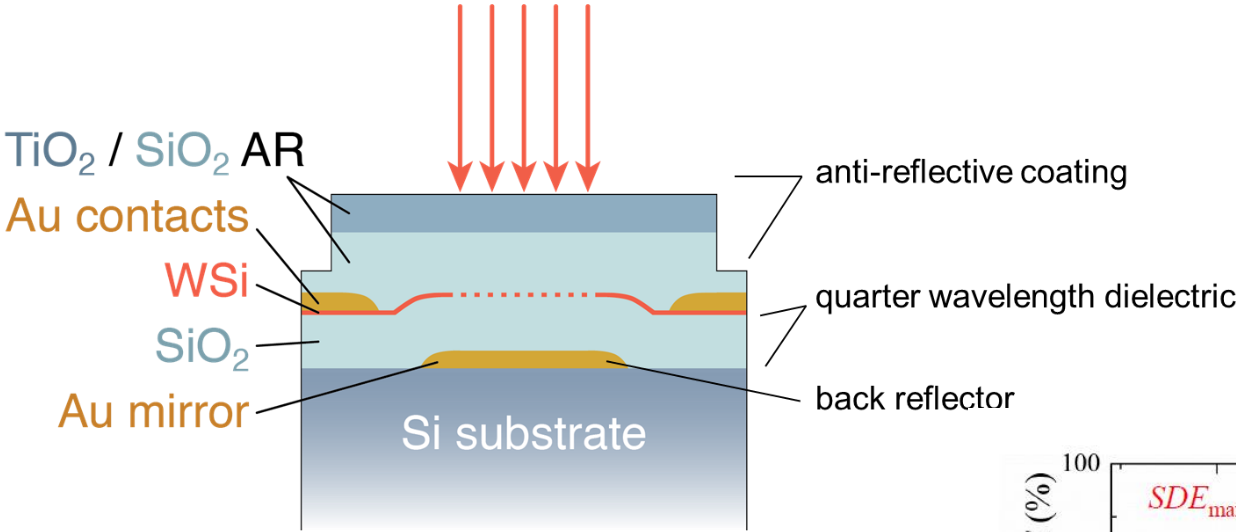
DSOC Project Overview

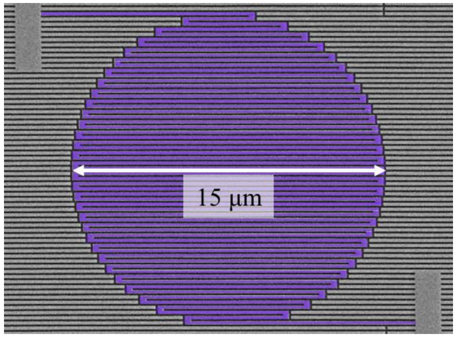
- Phase B of NASA Technology Demonstration Mission
- JPL flight terminal planned to launch on Psyche mission in 2022
- Projected downlink data rates from 200 kbps - 265 Mbps
- PPM 16 – 128, 500 ps – 8 ns slot widths, 4 slot intersymbol guard time
- Using a 320-µm 64-pixel WSi SNSPD array for the ground receiver



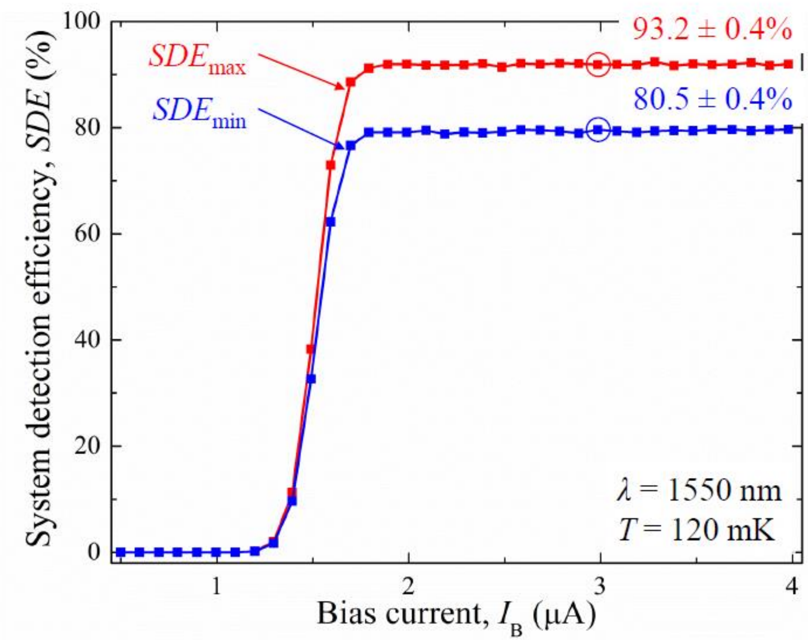
WSi SNSPD Architecture

NIST





- Photosensitive nanowire element is embedded in a vertical quarter-wave cavity
- Similar architecture developed by JPL and NIST in 2012 for single-pixel SNSPDs with 93% system detection efficiency
- Amorphous material allows scaling to 64-pixel arrays with high yield

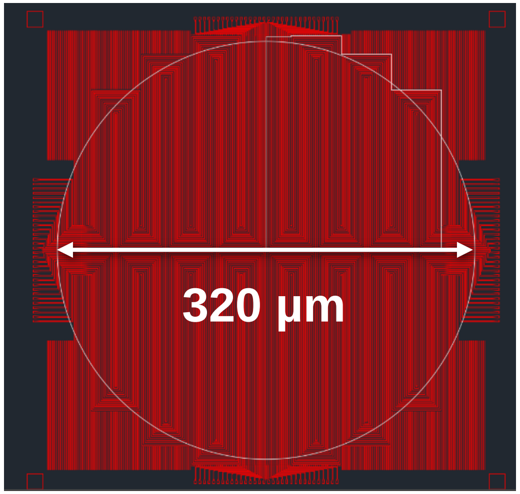


System detection efficiency for single pixel device

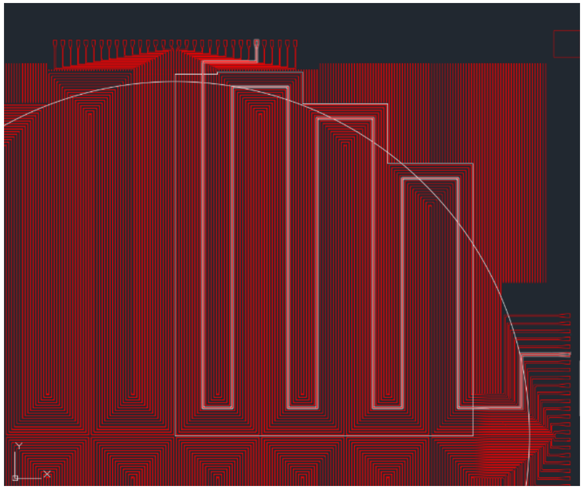
Marsili et al, *Nature Photonics* **7**, 210 (2013)

64-Pixel SNSPD Array for DSOC

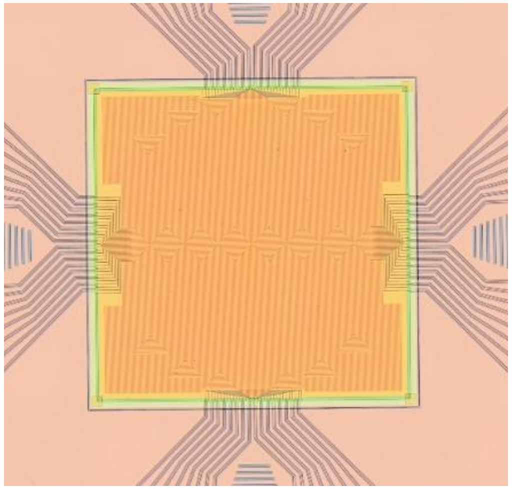
- 64-pixel WSi SNSPD array embedded in optical cavity optimized for 1550 nm
- 320-µm dia. free-space coupled active area, 4 quadrants, 16 co-wound wires per quadrant
- 13.3% nanowire fill factor: 4.5 x 160 nm wires on a 1.2 µm pitch
- Two-layer AR coating to enhance efficiency at low fill factor: 75% system detection efficiency
- 62 out of 64 measured nanowires show bias plateau
- Full 64-channel readout system and 64-channel time-to-digital converter



CAD Design of SNSPD focal plane array



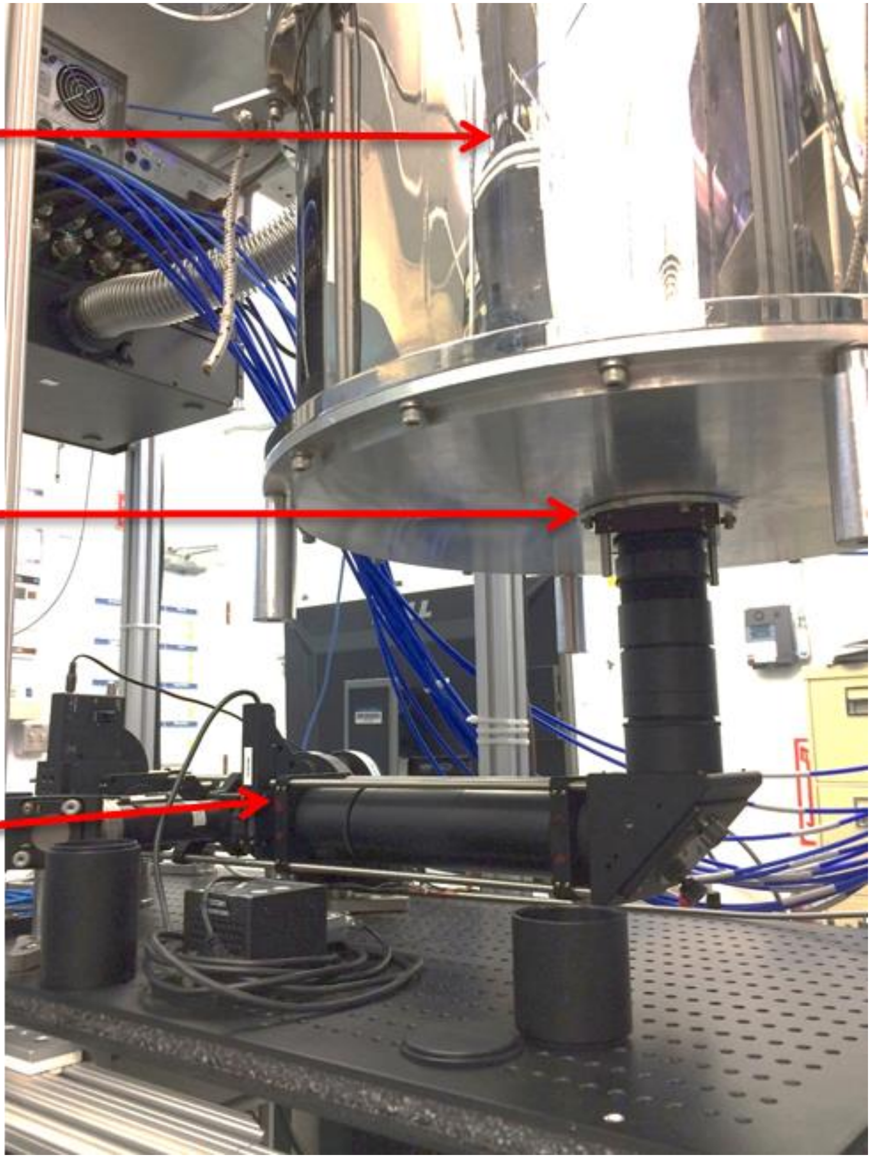
CAD Design showing one of 16 individual sensor elements per quadrant



Optical microscope image of SNSPD array

Free Space Coupling

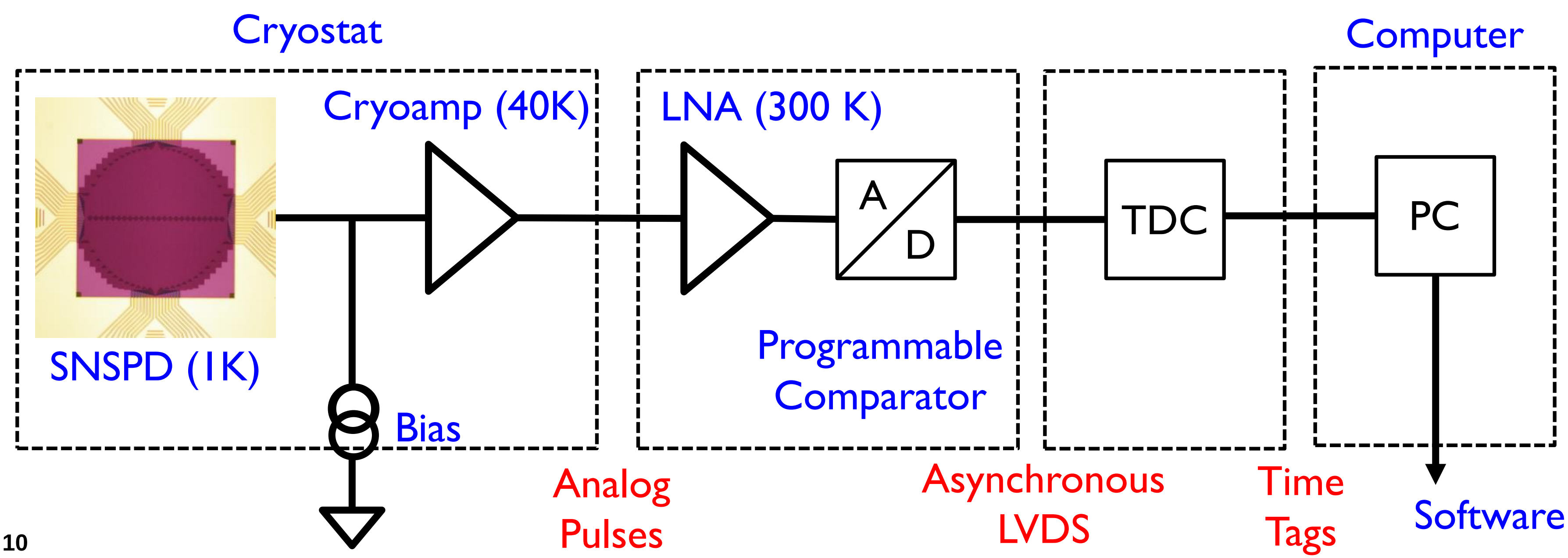
- Efficient coupling to large apertures requires free space coupling with cryogenic lens
- 300 K BK7 vacuum window
- 40 K, 4 K BK7 filters to block thermal background
- Engineering tradeoff between efficiency and false counts
- Experimenting with cryogenic spectral and spatial filters
- Must consider finite numerical aperture of detector



SNSPD Array Readout Architecture

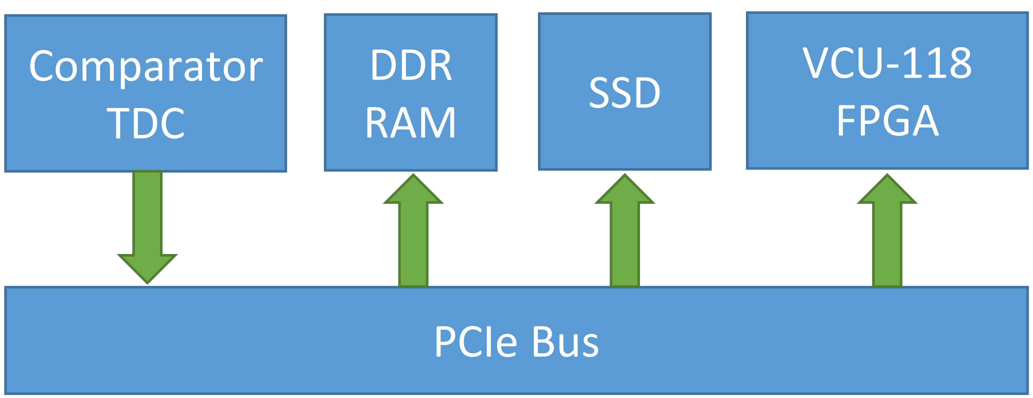
- Direct readout of 64 channels into an FPGA
- Brass flex circuits from < 1 – 40 K
- DC-coupled cryogenic amplifiers
- Copper flex circuits from 40 - 300 K
- Room temperature amplifiers and comparators
- FPGA-based time tagger
- Set up SNSPD optical communication testbed with flight-like transmit emulator

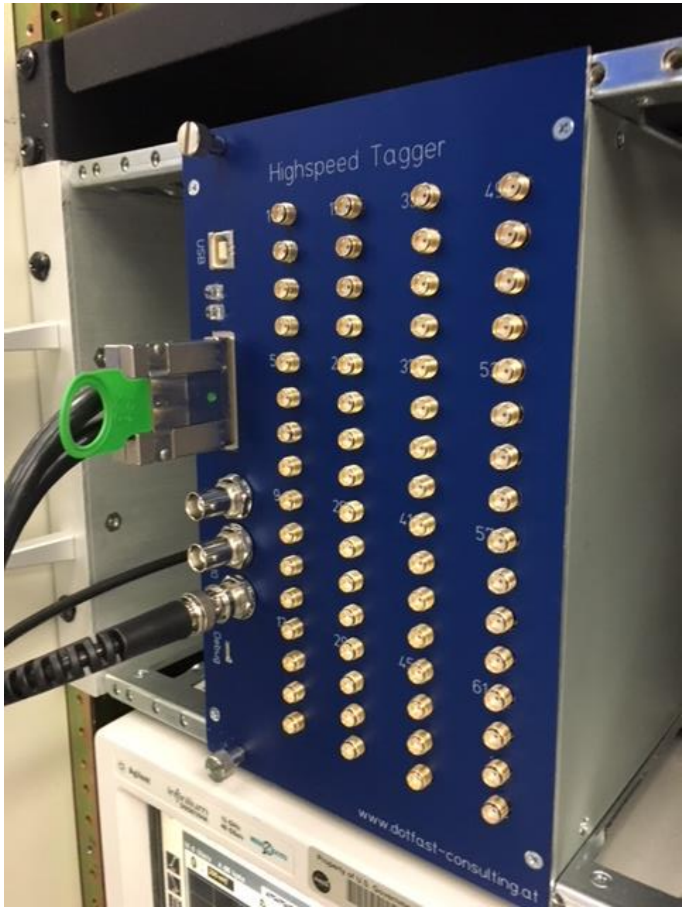
16-channel brass RF flex circuit



Time to Digital Converter Development

- Recently worked with outside consultant to develop high-rate 64-channel streaming time tagger
- Asynchronous time tagging across 64 independent channels
- < 30 ps single-shot timing jitter
- Demonstrated streaming 860 Mtps over PCIe
- Demonstrated streaming to memory, FPGA, SSD
- Each channel has integrated comparator front end

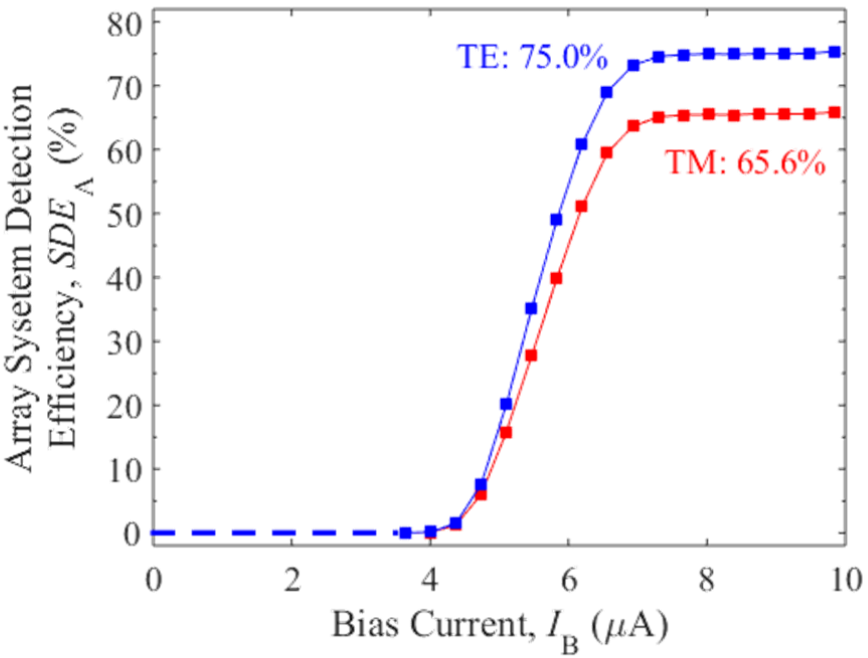




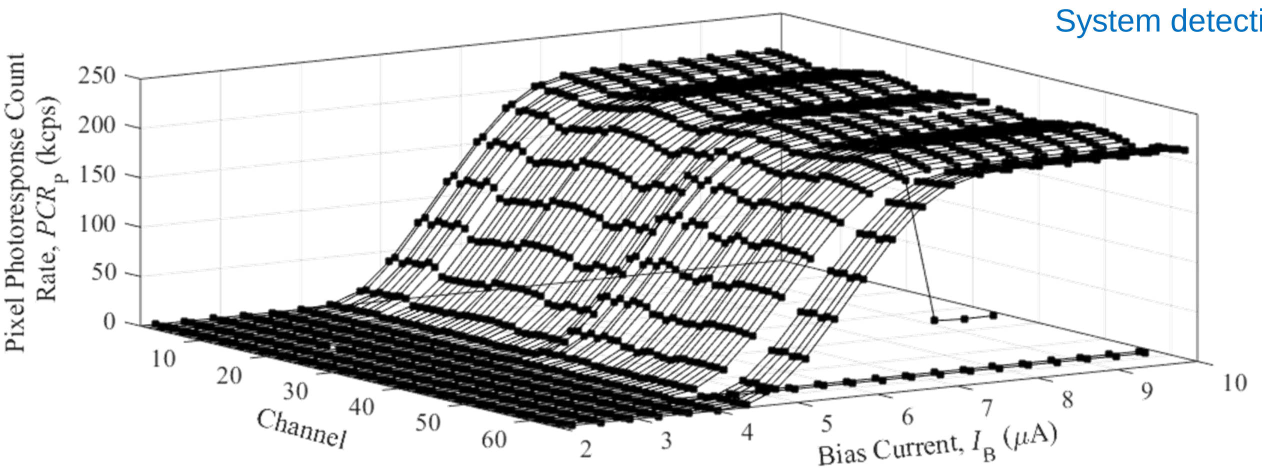
Streaming 64-channel time-to-digital converter

Efficiency Measurements

- 75% efficiency in TE polarization at 1550 nm, 66% in TM polarization
- System detection efficiency including coupling losses through cryostat window, 40K and 4K IR filters
- 62 out of 64 nanowires show bias plateau



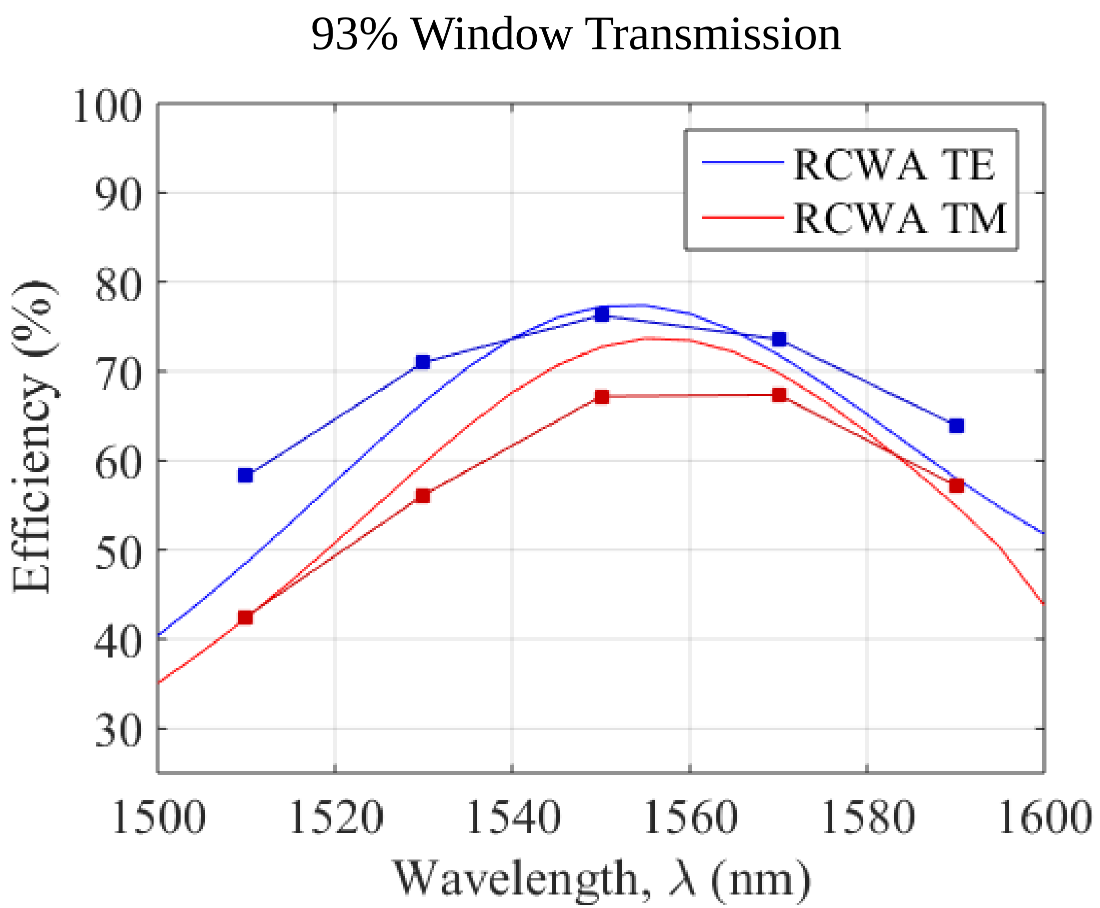
System detection efficiency across entire array



Photon count rate vs bias showing plateau on 62 nanowires

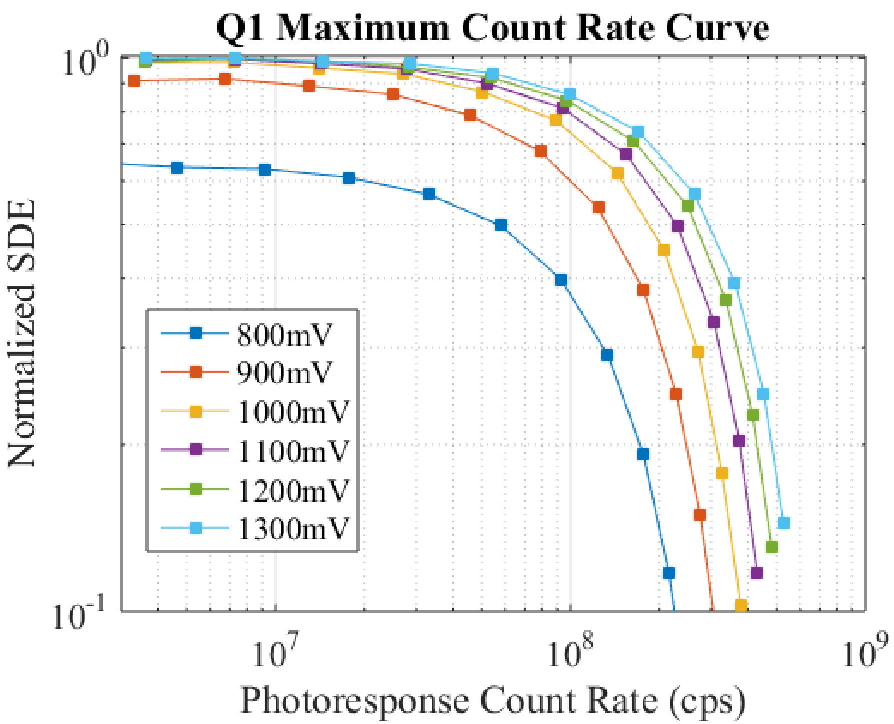
Efficiency Measurements

- Cavity is well centered near 1550 nm
- Efficiency matches RCWA simulation assuming 93% total transmission (97.6% per element)

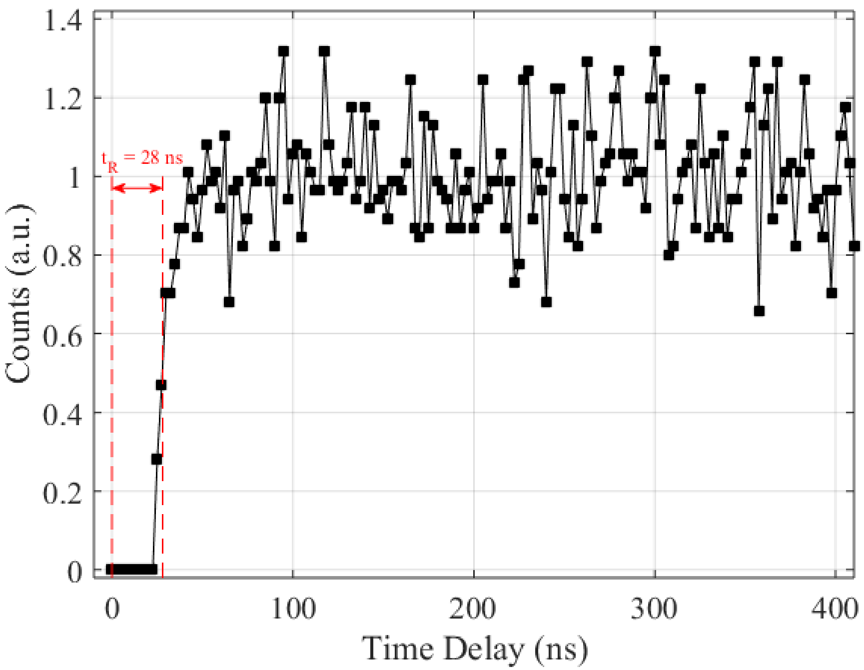


Wavelength dependence of system detection efficiency in both polarizations

Maximum Count Rate



Maximum count rate measured for one 16-channel quadrant

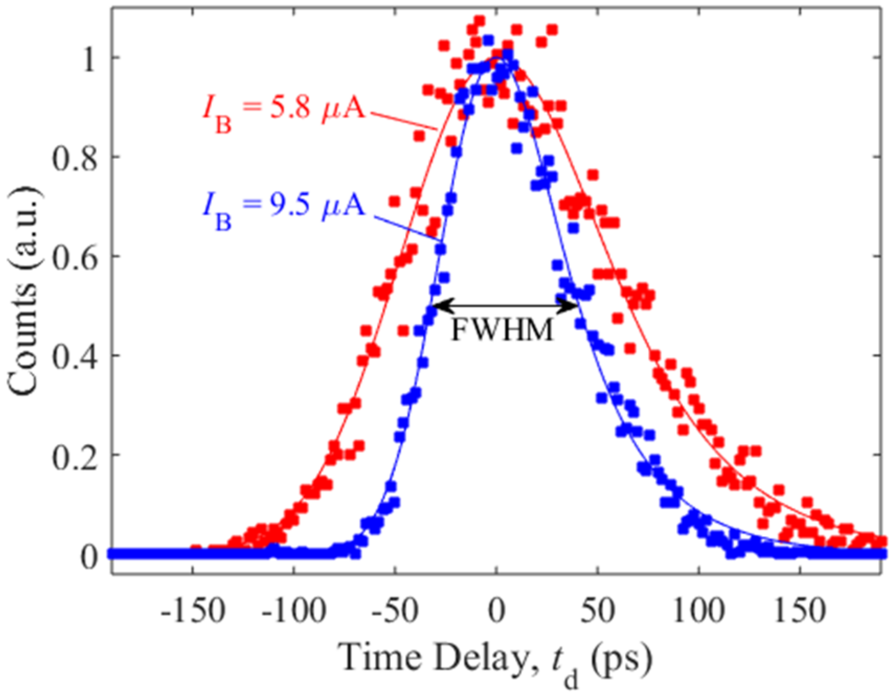


Interarrival time histogram showing 28 ns dead time, no afterpulsing

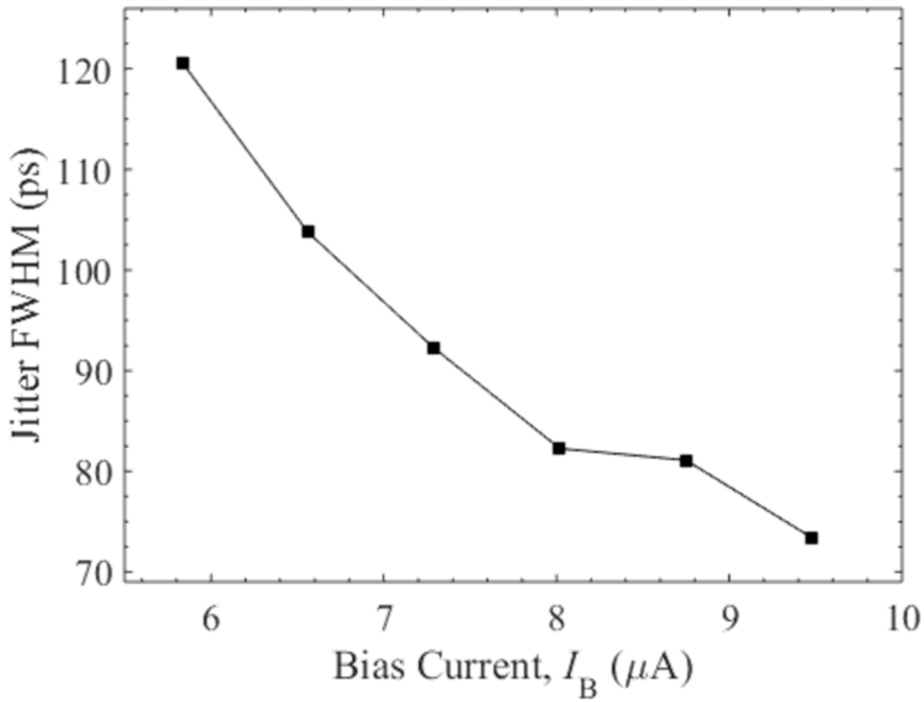
- MCR measured with beam centered on a single quadrant due to count rate limitations in TDC
- 120 – 300 Mcps 3dB point per quadrant
- Scales to 465 – 1160 Mcps across 62 pixels
- Present total counting rate is limited to 860 Mcps by time tagging electronics

Device Timing Jitter

- Representative individual pixel timing jitter measured using mode-locked laser and oscilloscope
- Instrument Response Function fits exponentially modified Gaussian
- 125 – 79 ps FWHM
- Additional ~30 ps jitter added by TDC is negligible



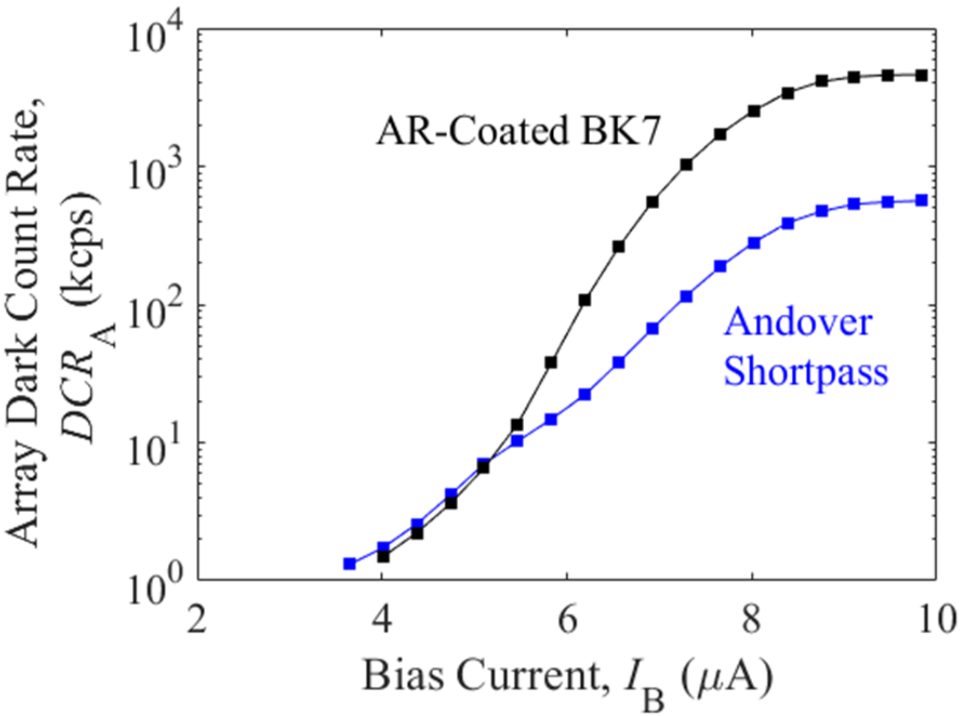
Timing jitter for one pixel of 64-pixel array



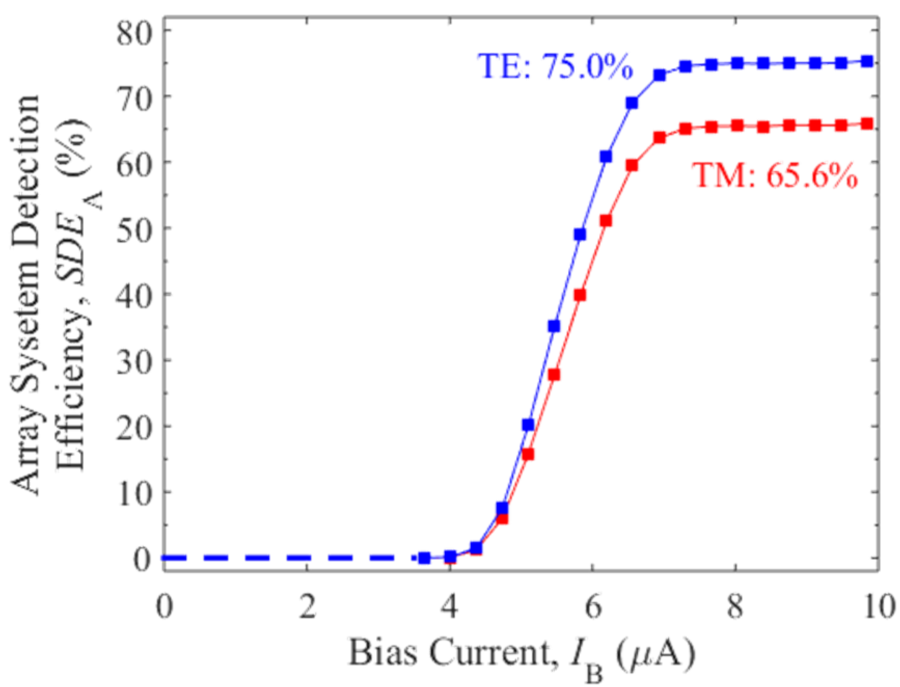
Dependence of jitter on bias current

False Count Rate

- 100 – 550 kcps false count rate across entire array, depending on bias point
- False counts are limited by blackbody IR loading from room-temperature optical system
- False counts in any individual application depend on etendue of optical system
- Blanked false counts are ~ 1 cps across array
- Bias dependence arises from changing mid-IR cutoff: 2.6 - 4.2 μm across plateau
- Cryogenic filters at 4K and 40K shields are used to reduce the mid-IR blackbody loading

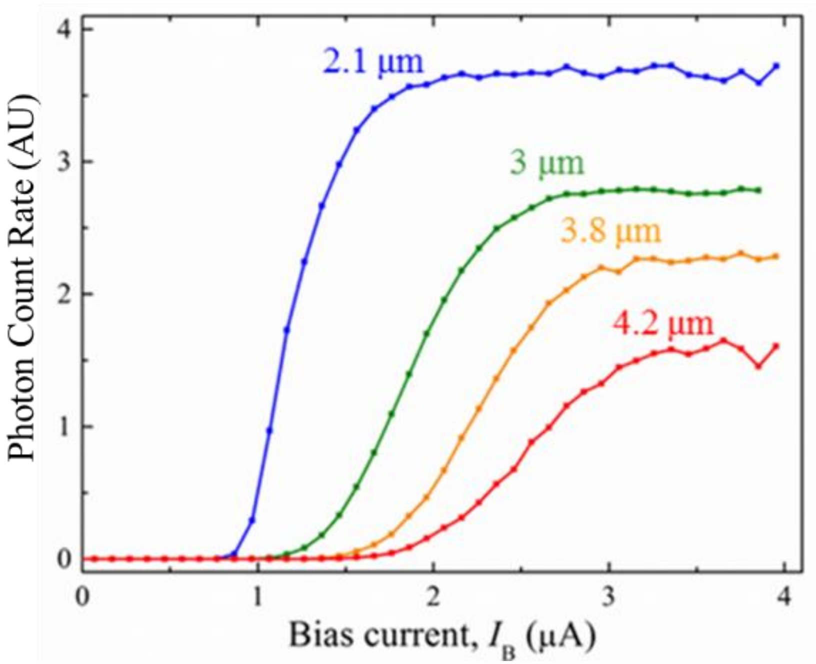


False counts across entire array under two different filter configurations



System detection efficiency as a function of bias

Mid-IR Response of WSi SNSPDs



Mid-IR response of 100 nm WSi SNSPD @ 120 mK
Courtesy M. Stevens and F. Marsili, NIST

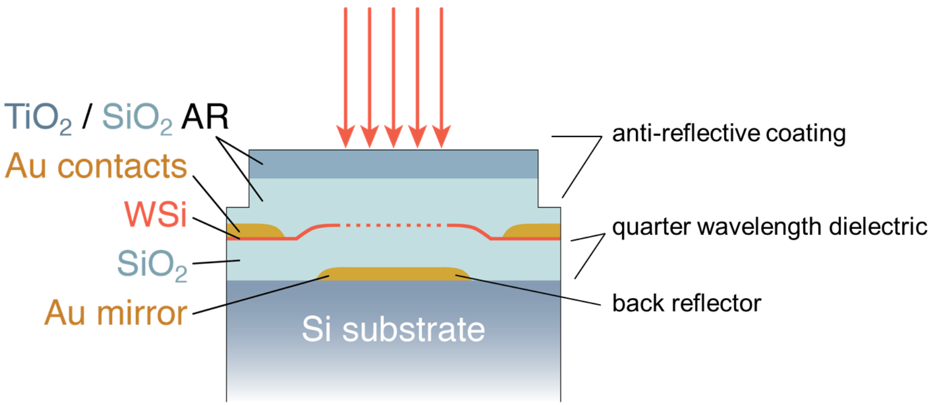
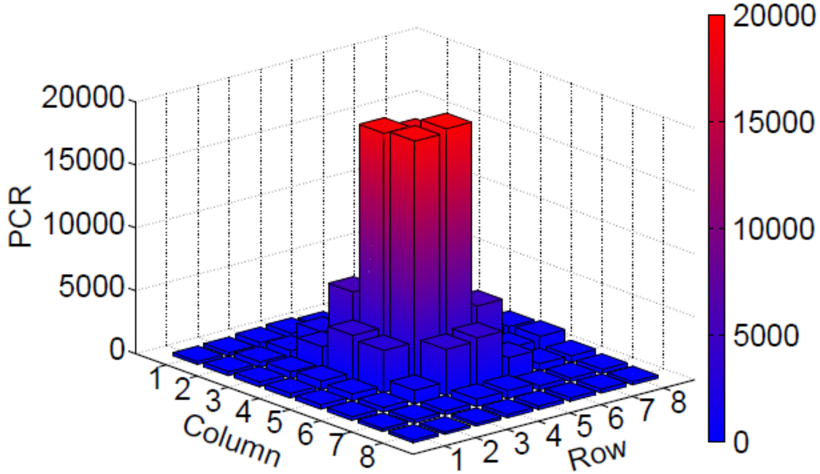


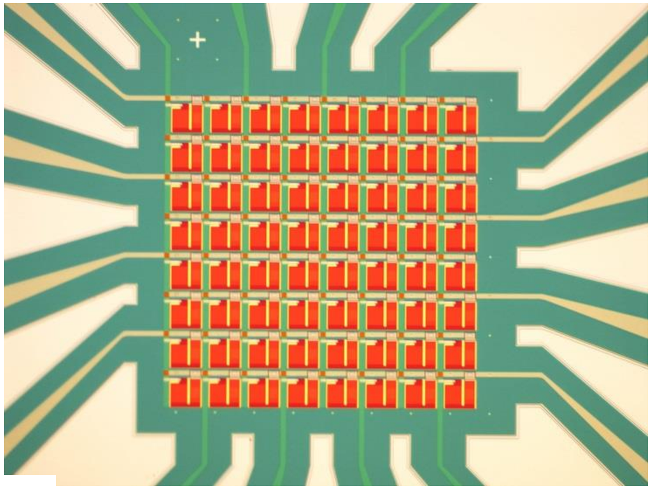
Illustration of quarter-wave optical stack concept

- High-efficiency SNSPDs can be engineered throughout the mid-IR
- WSi SNSPD shows bias plateau to 4.2 μm – stack can be engineered for high efficiency
- Single photon sensitivity recently demonstrated at 9.9 μm at JPL using cryogenic QCL

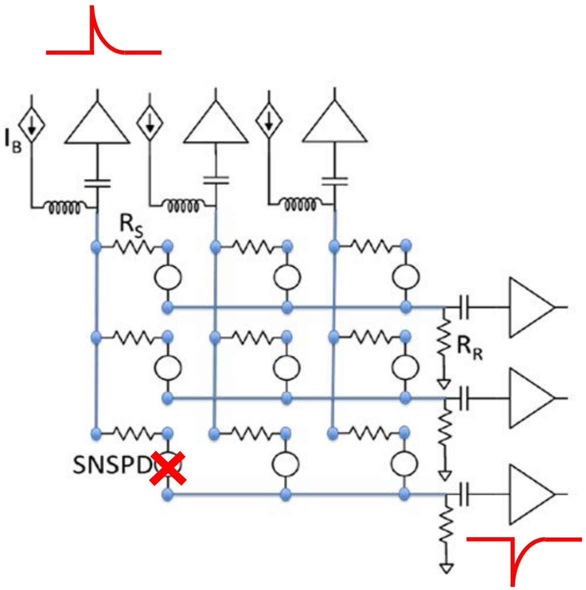
64 Pixel "Row-Column" Arrays



- 64 pixel (8 x 8) sparse WSi SNSPD array for fast time-correlated imaging
- Row-Column readout strategy allows 64 pixels to be read out using 16 lines
- Collaboration between JPL and NIST
- Kilopixel Row-Column arrays are "low-hanging fruit" with 64-channel readout



8x8 Array at 1550 nm



Operating Concept

NIST

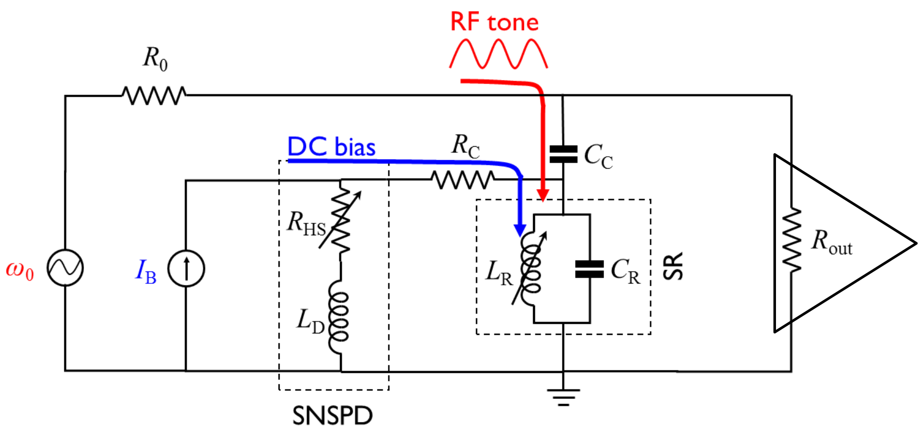
Allman et al, APL (2015)

Multiplexing Strategies for SNSPDs

Jet Propulsion Laboratory
California Institute of Technology

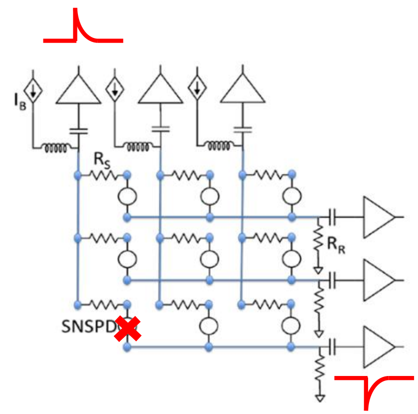
Frequency Domain

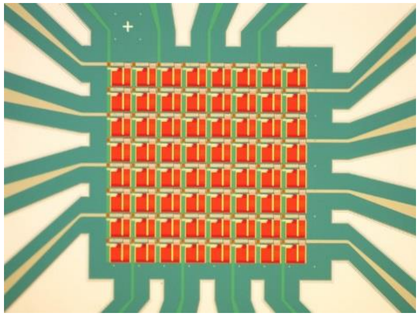
Karlsruher Institut für Technologie



- Similar trade space to MKIDs

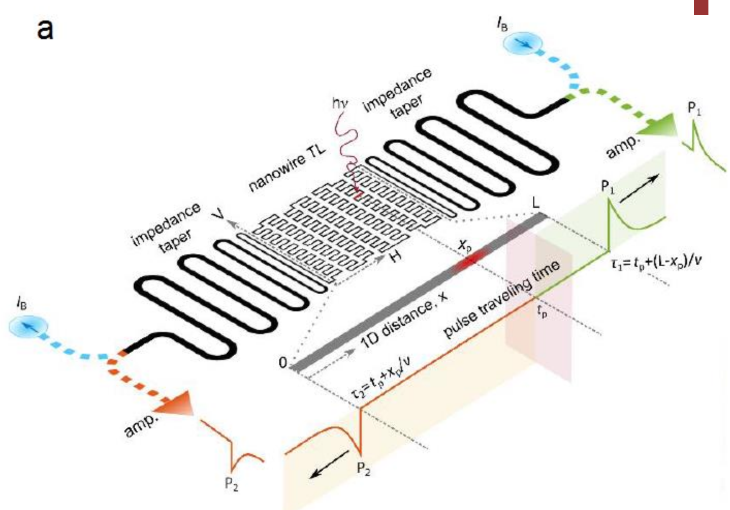
Row-Column



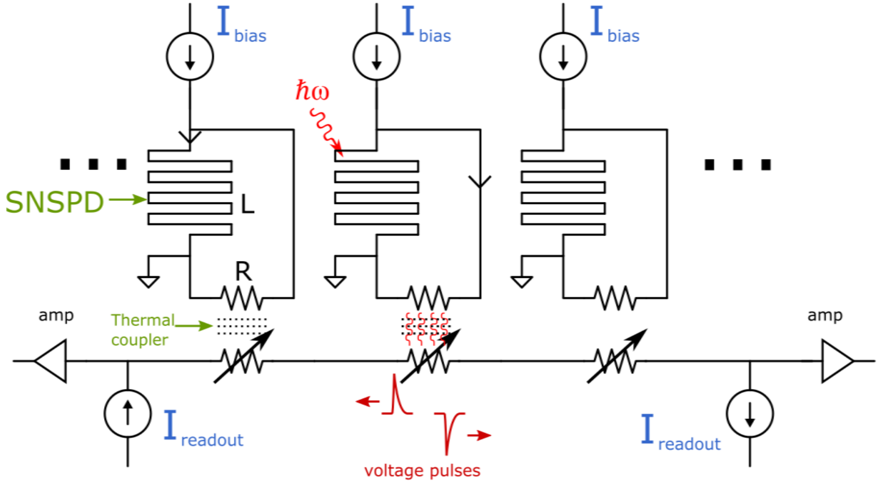


- NxN array read out with 2N readout lines

Position Sensitive Nanowire

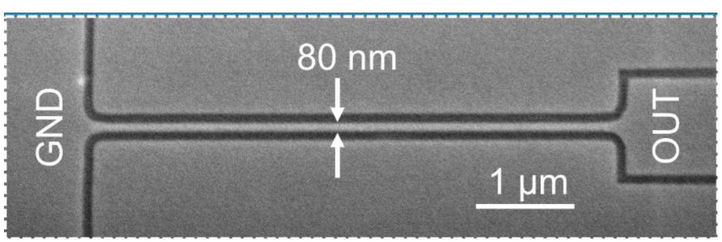


Thermally Coupled Imager

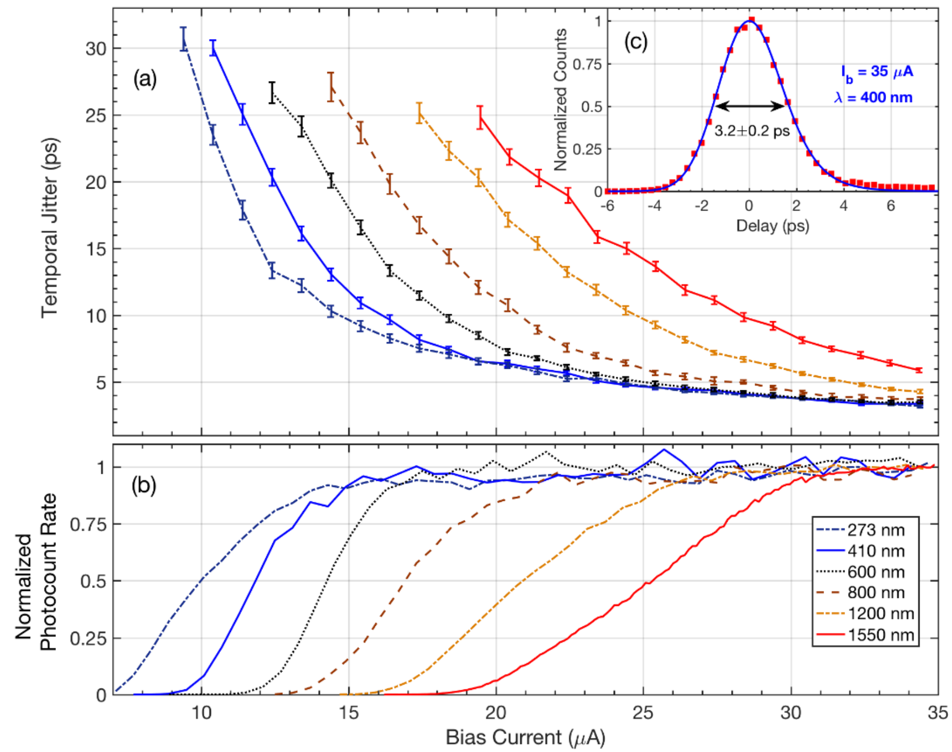


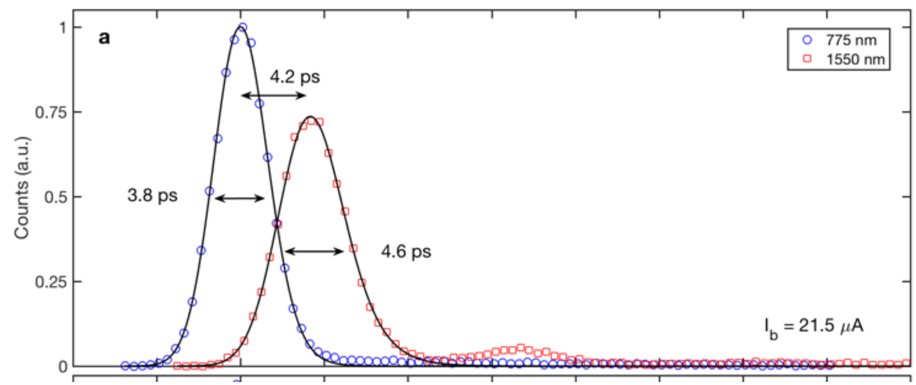
Ultra-high time resolution in SNSPDs

- Time resolution of SNSPD reduced from ~15ps to 3 – 5 ps FWHM
- Specialized device fabricated at MIT and tested at JPL
- Ultra-low-noise amplifier was used with high switching current SNSPD to maximize SNR
- Same setup with differential version of DSOC array yields 25 ps jitter
- Jitter depends on energy for the first time – provides laboratory for probing device physics



Specialized low-jitter NbN SNSPD

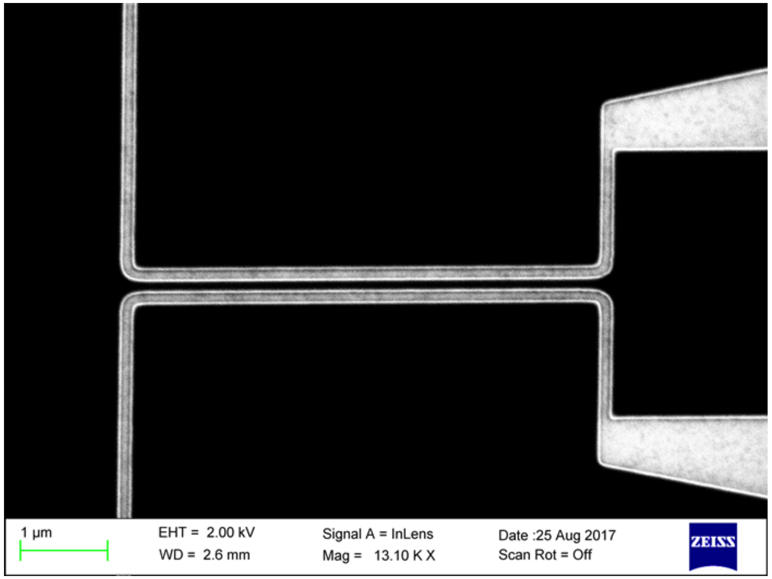


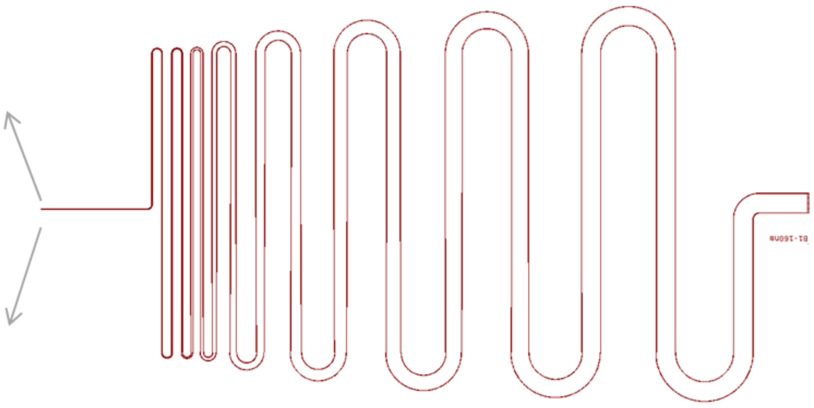


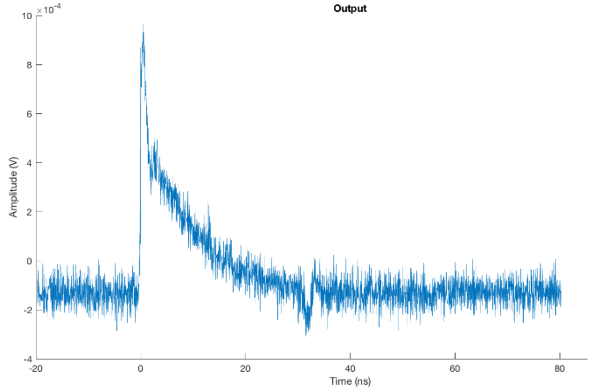
Dependence of timing jitter on photon energy

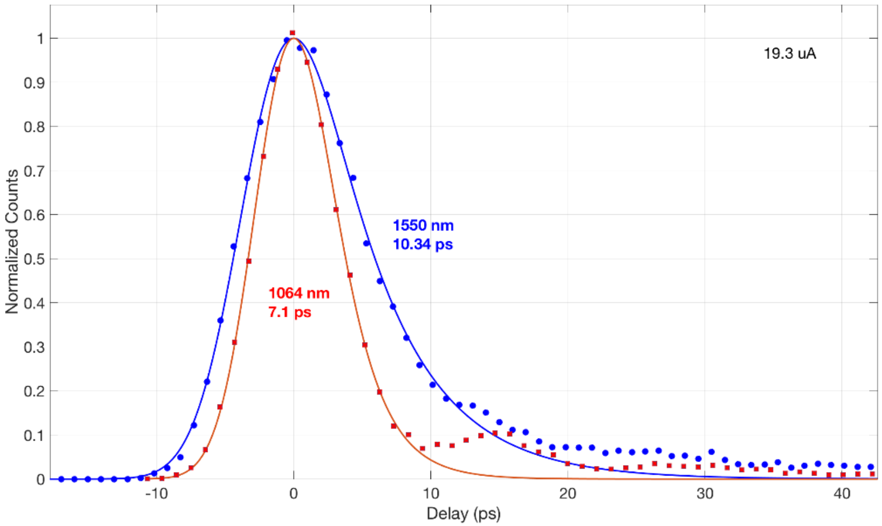
7ps Jitter with WSi

Jet Propulsion Laboratory
California Institute of Technology





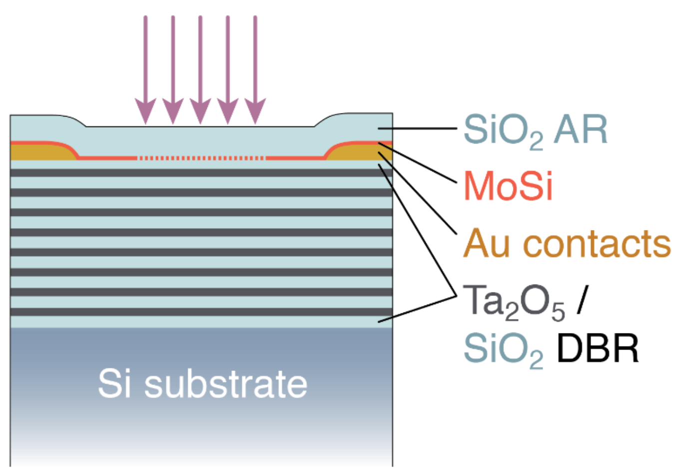


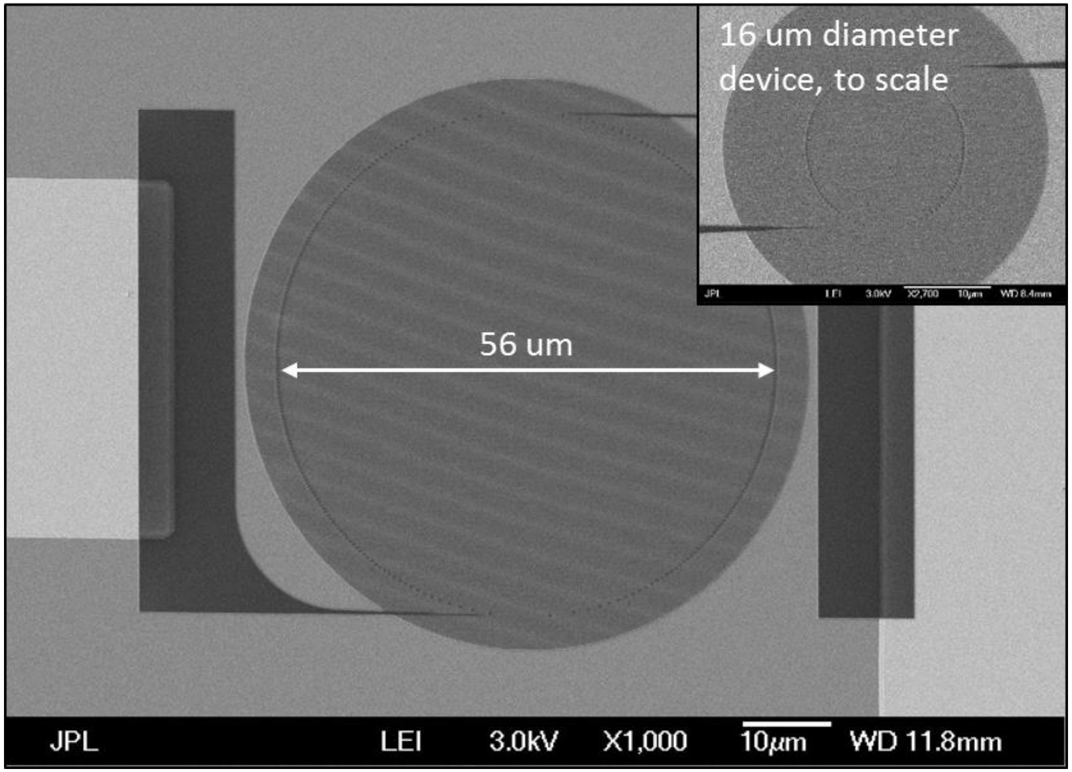


- Device fabricated at MIT with JPL WSi
- Taper matches impedance to 50Ω to improve SNR
- No amplifier required! ~1 mV signal

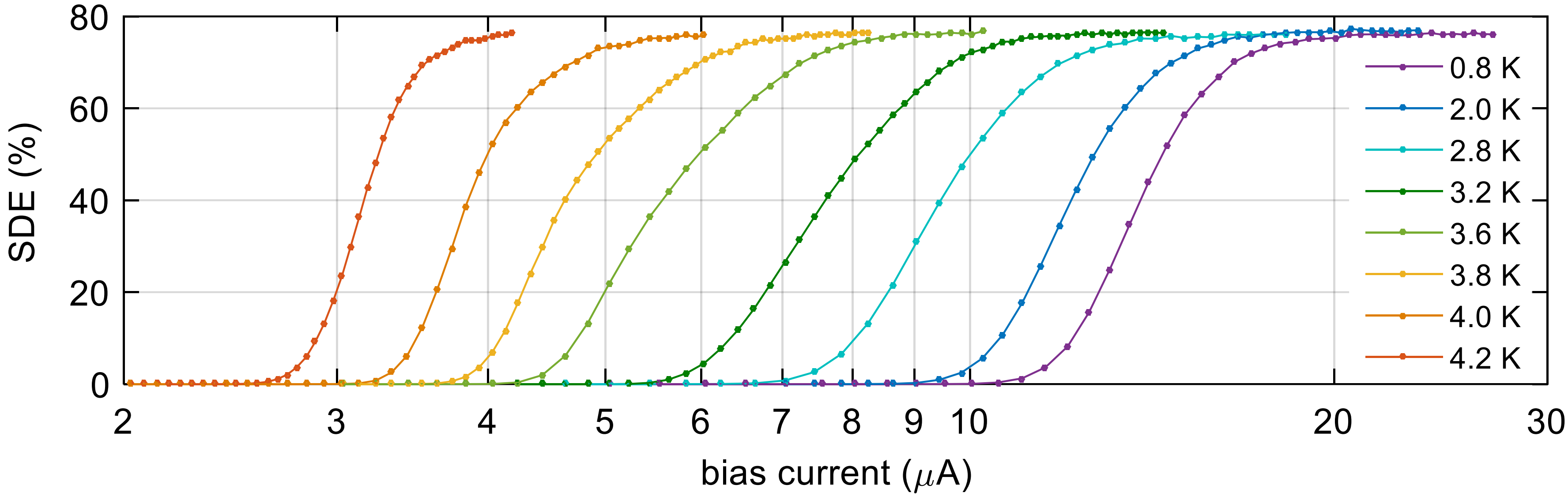
Ultraviolet SNSPDs

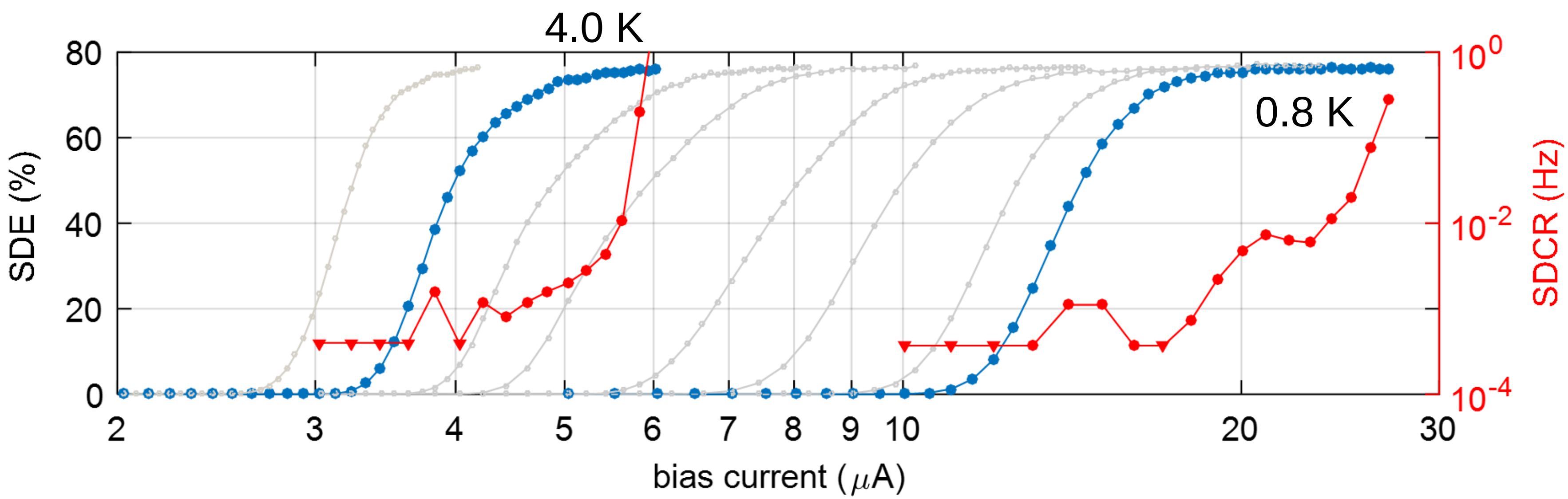
- Fiber-coupled MoSi UV SNSPDs for applications in ion trap quantum computing
- 80% Efficiency at 370 and 315 nm, single photon sensitivity at 245 nm
- DBR mirrors to enhance absorption
- 4.2 K operating temperature
- mHz dark count rates when coupled to optics, < 7e-5 cps intrinsic dark count rates



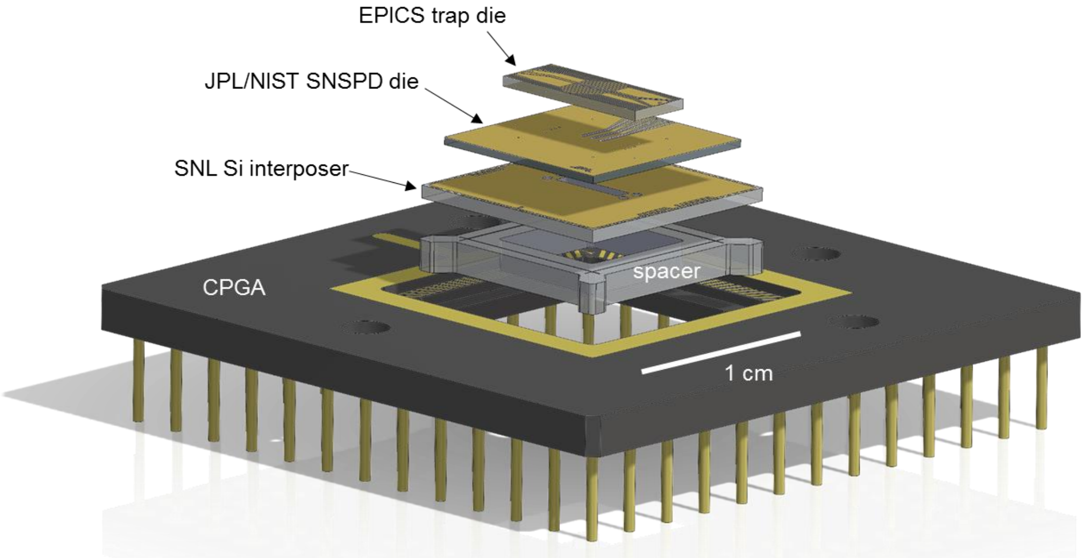


Efficiency and Dark Counts at 370nm

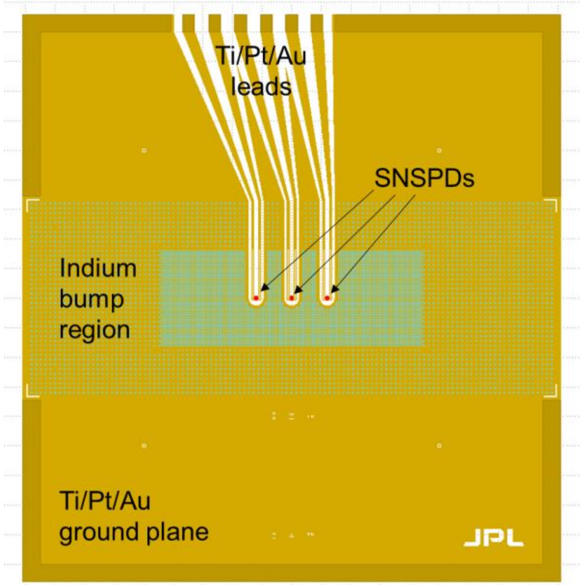


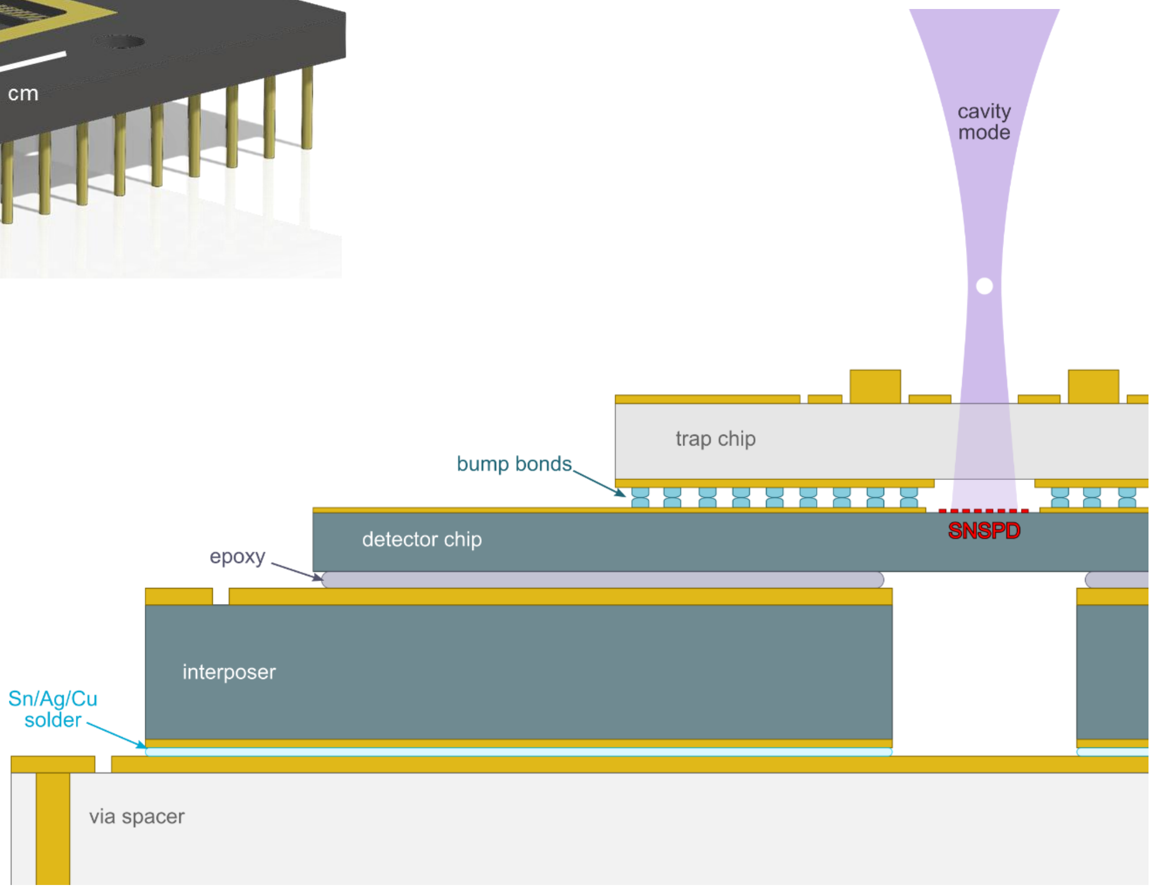


Integration with Ion Trap Chips



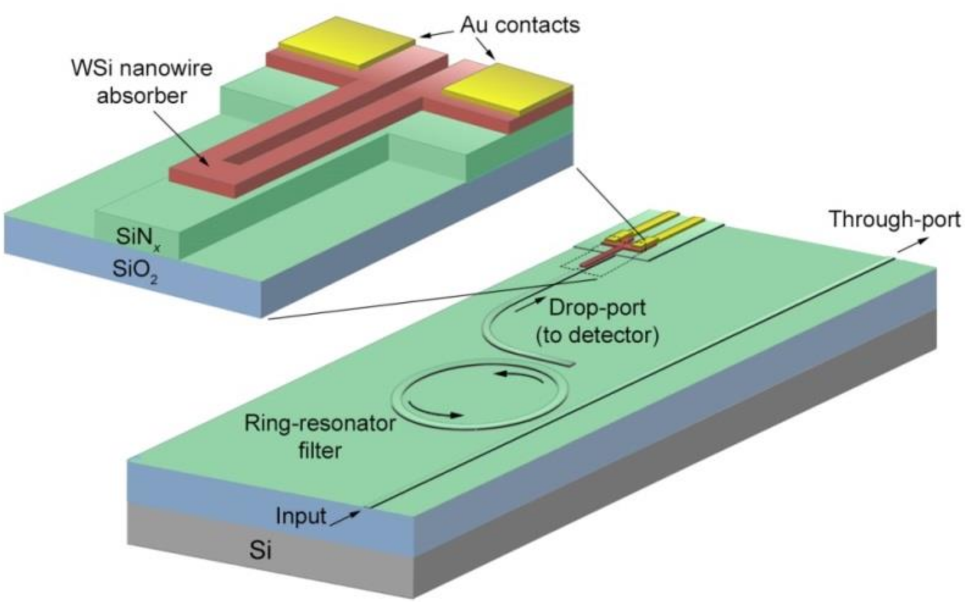
- Hybrid integration between ion trap chips and free-space UV SNSPDS
- Collaborative effort between JPL, NIST, Sandia, and Duke University

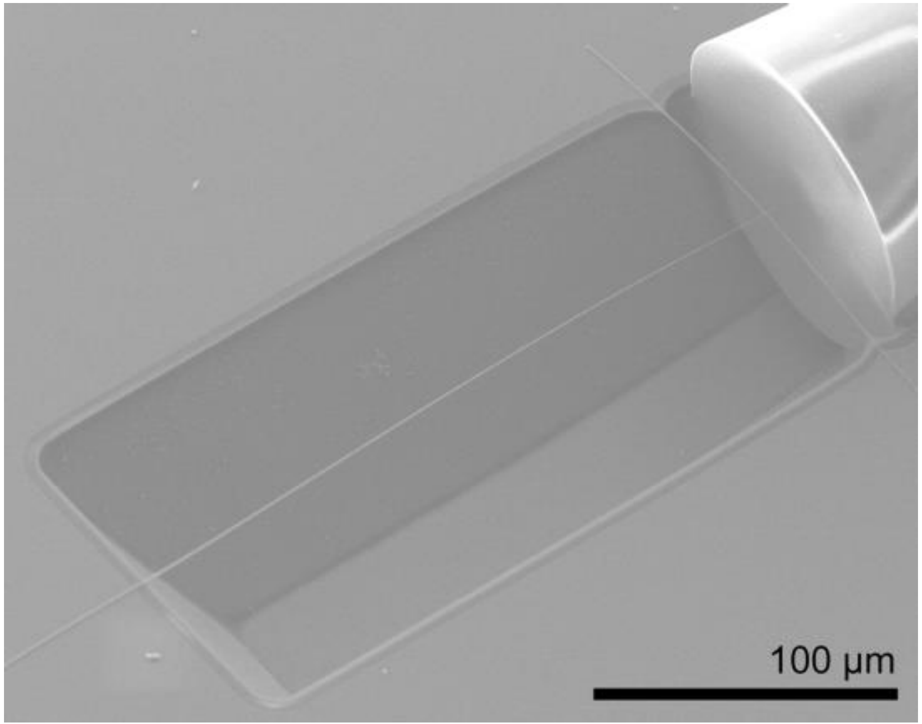




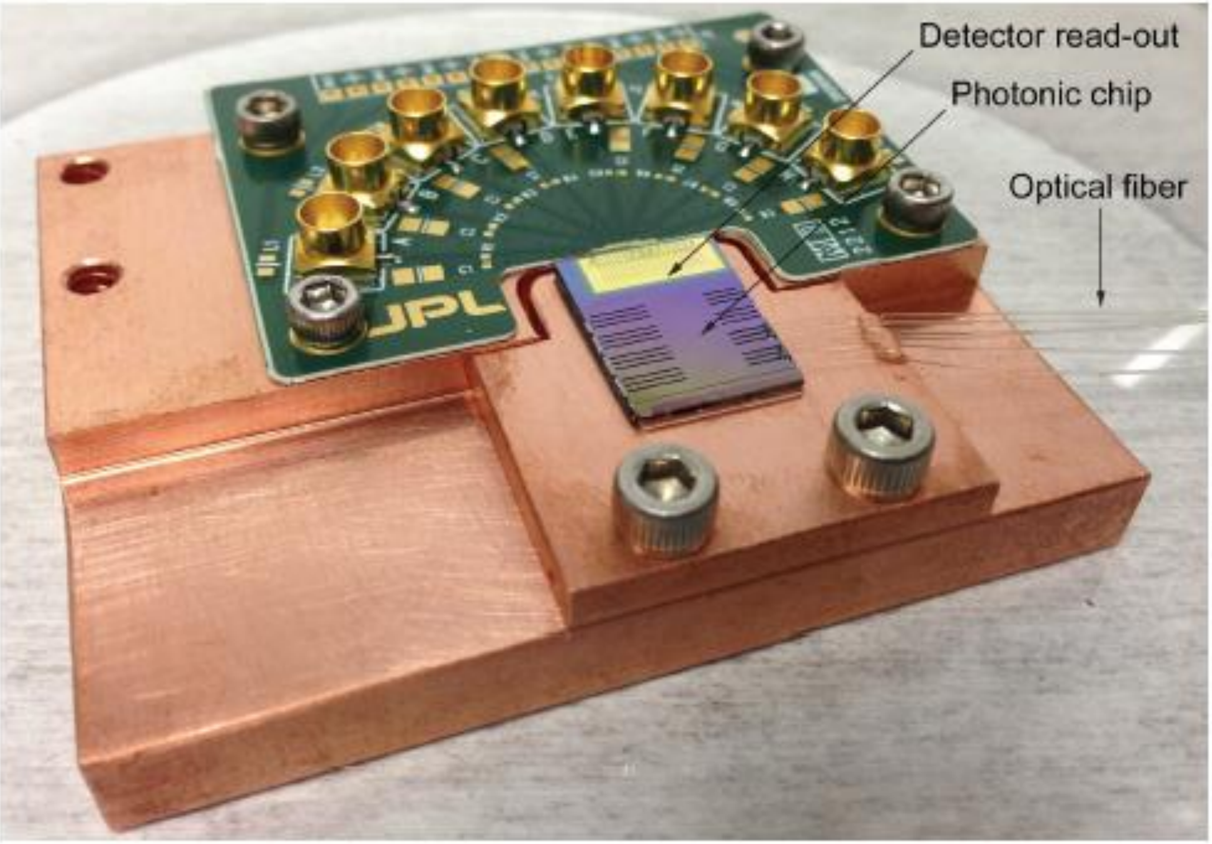
On-Chip Integrated SNSPDs

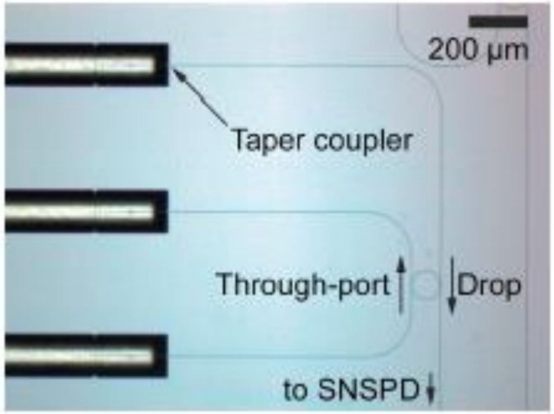
- WSi SNSPDs coupled to SiN waveguide photonics platform
- Integration with low-loss broadband optical couplers (Collaboration w/ Painter Group, Caltech)
- Integration with on-chip ring resonators or echelle grating to form channelizing spectrometer or DWDM receiver for QKD
- Can realize a robust, on-chip cryogenic spectrometer, particularly in the mid-IR
- Promising preliminary results

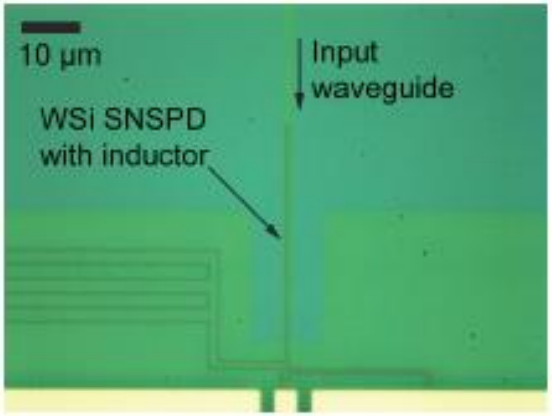




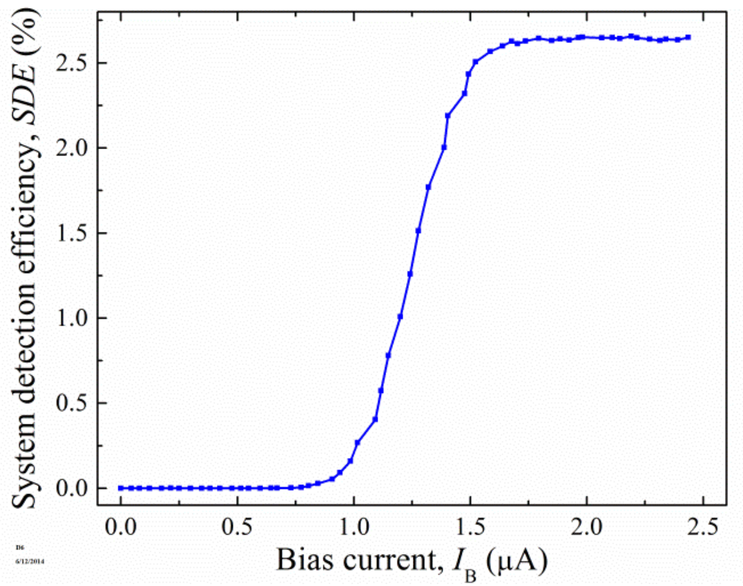
On-Chip Integrated SNSPDs

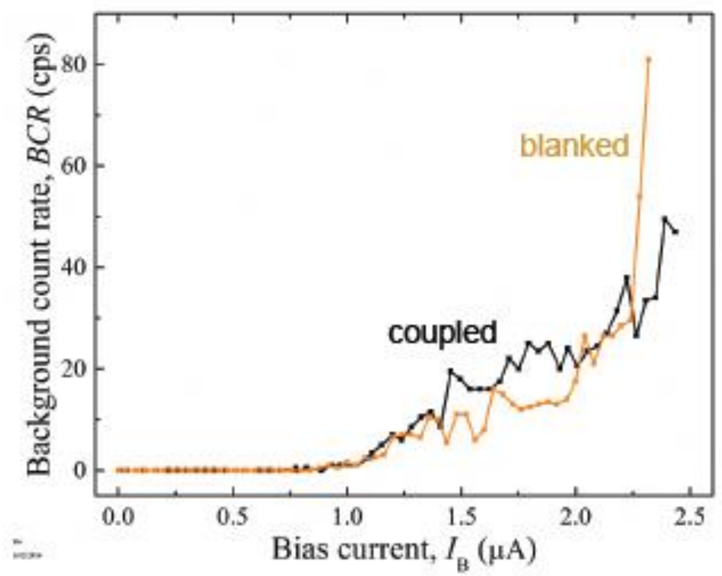


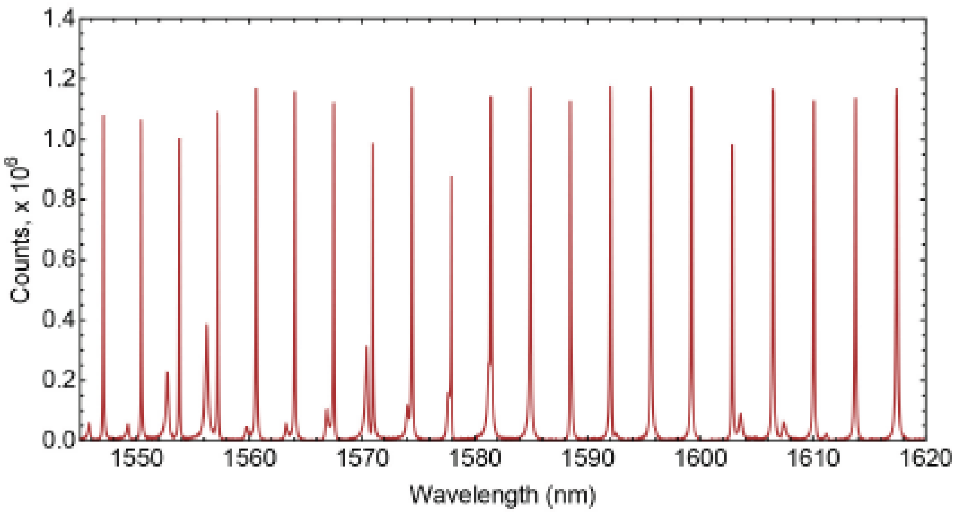


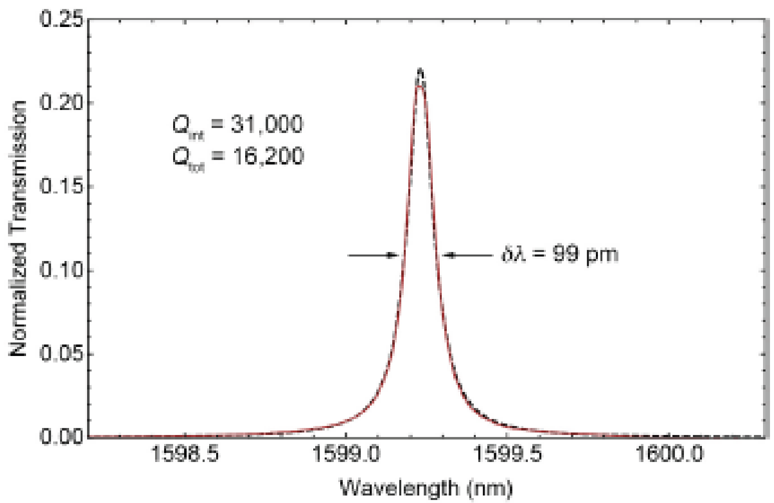


On-Chip Integrated SNSPDs



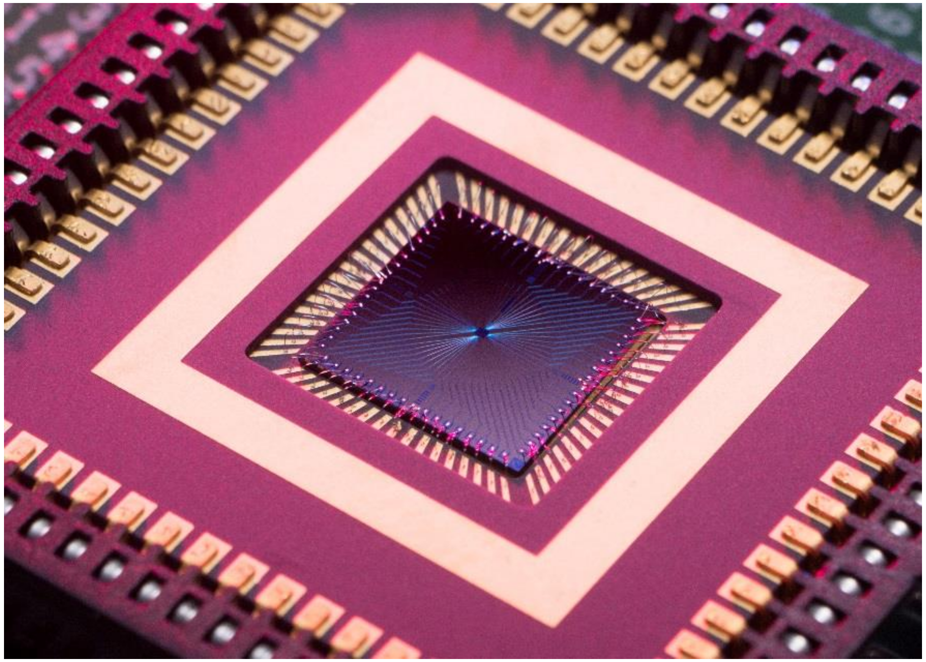




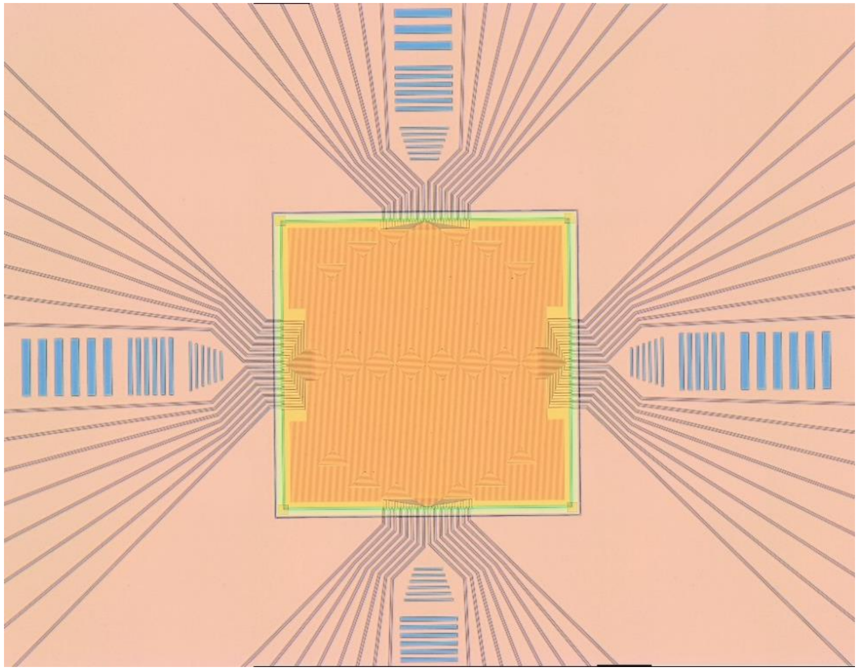


Conclusions

- SNSPDs are the highest performing detectors available for time correlated single photon counting
- They are enabling the first true demonstration of optical communication from deep space
- Progress in performance has been extremely rapid
- Technology is very new, with many opportunities for new innovation
- Many open directions for exploring new applications and new device concepts



64-pixel SNSPD array mounted in chip carrier



Optical microscope image of array